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A USB 3.0 readout system for Timepix3 detectors with on-board processing capabilities

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ABSTRACT: Timepix3 is a high-speed hybrid pixel detector consisting of a 256x256 pixel matrix with a maximum data rate of up to 5.12 Gbps (80 MHit/s). The ASIC is equipped with eight data channels that are data driven and zero suppressed making it suitable for particle tracking and spectral imaging.

In this paper, we present a USB 3.0-based programmable readout system with online pre-processing capabilities. USB 3.0 is present on all modern computers and can, under real-world conditions, achieve around 320 MB/s, which allows up to 40 MHit/s of raw pixel data. With on-line processing, the proposed readout system is capable of achieving higher transfer rate (approaching Timepix4) since only relevant information rather than raw data will be transmitted.

The system is based on an Opal Kelly development board with a Spartan 6 FPGA providing a USB 3.0 interface between FPGA and PC via an FX3 chip. It connects to a CERN TIMEPIX3 chipboard with standard VHDCI connector via a custom designed mezzanine card. The firmware is structured into blocks such as detector interface, USB interface and system control and an interface for data pre-processing. On the PC side, a Qt/C++ multi-platform software library is implemented to control the readout system, providing access to detector functions and handling high-speed USB 3.0 streaming of data from the detector.

We demonstrate equalisation, calibration and data acquisition using a Cadmium Telluride sensor and optimise imaging data using simultaneous ToT (Time-over-Threshold) and ToA (Time-of-Arrival) information. The presented readout system is capable of other on-line processing such as analysis and classification of nuclear particles with current or larger FPGAs.

1 Introduction

1.1 Timepix3

The TIMEPIX3 chip is a hybrid pixel detector developed by the Medipix group at CERN and currently one of the most advanced spectral imaging/photon counting devices available. It consists of a 256×256 pixel matrix with a pixel pitch of $55 \mu\text{m}$. Every pixel can be configured in three modes: *Time-over-Threshold* (ToT) with simultaneous *Time-of-Arrival* (ToA), ToA only or photon counting with integrated ToT (iToT). The maximum hit rate is at around 85 MHit/s [1], which translates to a data rate of 5.12 Gbps [2, 3]. For more efficient data readout a zero-suppressed and event-driven streaming architecture is used.

Due to the high speed and data rate, the TIMEPIX3 is suitable for particle tracking, neutron measurements and spectral imaging applications [4]. Furthermore, the detector can be used for medical applications as well [5, 6].

1.2 Readout Systems

Due to the chip's design, an FPGA is required to handle the detector output. Pre-processing of the raw data is highly beneficial to reduce strain on the readout computer and to reduce the time spent on post-processing. Also, it can contribute to saving costs by allowing to use standard hardware. All outputs are *scalable low-voltage differential signalling* (SLVS) signals, which cannot be utilised directly by most FPGA's. Therefore, level converters are required shifting the signals to *low-voltage differential signalling* (LVDS) level [2, 3]. The selection of a host interface is limited by the high data rate. USB 3.0 can theoretically achieve up to 5 Gbit/s (625 MB/s) and is present on most modern computers making it a favourable choice for a readout system, while 10 Gbit Ethernet requires additional hardware for communication and 1 Gbit Ethernet would limit the bandwidth. However, considering the protocol overhead, the maximum achievable data rate via USB 3.0 is expected to be around 320 MB/s.

Commercially available readout systems for TIMEPIX3 are SPIDR (LynX 1800) [7, 8], AdvaDAQ [9], and Katherine [10]. However, these systems did not grant firmware access, thus preventing the implementation of on-board processing.

The presented readout system allows access to the FPGA and thereby to implement on-board processing algorithms, such as filtering, clustering, and compression [11]. Pre-processing of data is becoming a crucial approach for usability of TIMEPIX3 detectors. Considering the data rate increase expected for Medipix4, pre-processing will become inevitable for many applications.

2 System Design

The readout system (Figure 1) consists of a prototyping board, a mezzanine card, FPGA firmware, and a desktop control library. As prototyping board, the XEM6310 from Opal Kelly was selected. It provides a Xilinx Spartan-6 FPGA with sufficient IO and a USB 3.0 interface via a Cypress FX3 ARM co-processor. The control library is implemented in C++ using Qt and can be compiled for Linux, MacOS, and Windows. A custom readout interface is built on top of the library.

2.1 Hardware

The mezzanine card is designed to connect a CERN TIMEPIX3 chipboard via a VHDCI connector and on the other side to the FPGA card with 2 SAMTEC connectors. Furthermore, it contains SLVS-to-LVDS level converters, a multi-channel *analogue-to-digital converter* (ADC), JTAG (an

industry standard named after the Joint Test Action Group) for debugging and power supply to the TIMEPIX3 chipboard.

2.2 Firmware

The FPGA firmware consists of several blocks: detector interface, USB interface, and firmware core (see Fig. 2). The firmware core includes pre-processing modules and an interface for more advanced on-board processing algorithms. Opal Kelly provides the FrontPanel framework including so called *HDL Endpoints* creating a connection between the FPGA and the host via an *application programming interface* (API). A configuration and debugging interface was implemented in the USB interface.

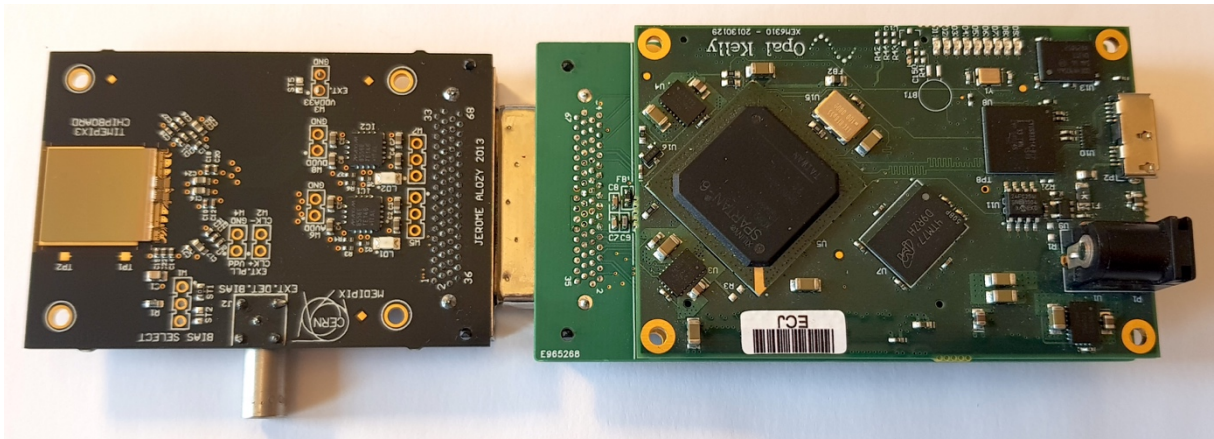


Figure 1: Photo of the developed readout system. Timepix3 detector on the standard CERN chip board on the left, custom adapter board with Opal Kelly XEM6310 development board on top on the right side.

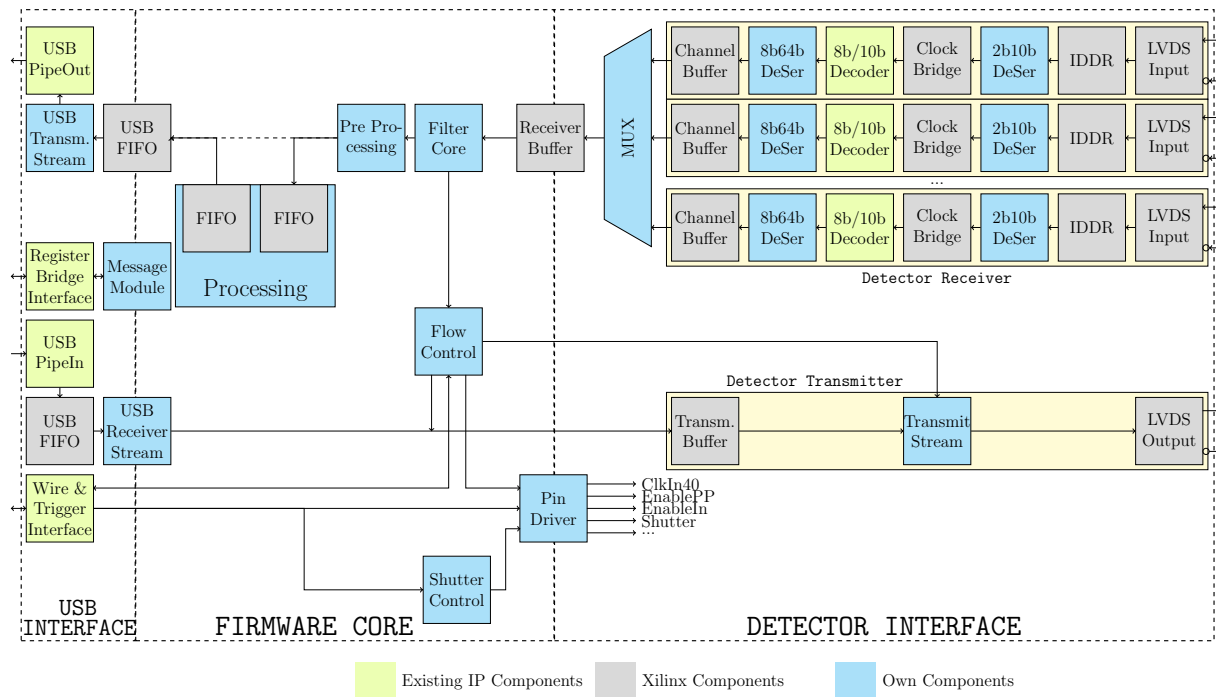


Figure 2: The firmware is structured into a detector interface, USB interface, and firmware core, which also contains pre-processing modules and an interface for processing modules.

The firmware core implements a `flow_control` module managing the data flow between the host and the detector. To identify the detector's control packets, the `filter_core` module was implemented scanning the headers of all received data packets. The detector's shutter is controlled by the `shutter_control` module for precise timing down to 1 μ s assuring independence from delays caused by the USB interface or the host.

The readout clock signal has to be taken into account to receive, de-serialise, and decode data from the detector. Furthermore, the detector interface supports clock recovery from the detector allowing the detector to generate the readout clock. Transmitting commands to the detector is implemented as a 40 MHz serialiser.

The USB interface implements streaming pipelines to receive and send data to the host. Time-critical status information can be transmitted from and to the device independently from the pipelines. Furthermore, detailed status and debug information are available via a configuration and debug interface. High-speed data streaming is controlled with an algorithm dynamically adjusting the streaming parameters of the FrontPanel pipelines.

2.3 Software

The library manages the readout system, allows to configure the TIMEPIX3 chip, send commands, and receive data via USB. It is implemented in C++ and Qt utilising the FrontPanel API. Different functionality was split into different classes, which are inherited to a base class. Implemented classes are: detector configuration, command creation, and readout communication.

For high-speed data streaming between readout system and host, an algorithm was designed automatically adjusting the streaming parameters. A two-buffer design was implemented handling simultaneous receiving and writing of data. One buffer is used to receive data, while the other is written to a file in a separate thread. When the receiver buffer is full, the threads exchange their buffers only causing a minimal delay.

3 System Verification

3.1 Equalisation and Calibration

The CdTe detector was equalised using noise centroids [12]. An energy calibration of the used CdTe detector was conducted using fluorescence energies [13]. Different samples were illuminated at a 45° angle and the resulting spectrum was captured with the detector. First, a calibration curve for the whole detector was created, then a calibration curve for every individual pixel was created resulting in a much more precise energy calibration.

3.2 USB 3.0 Data Streaming

Benchmarking the implemented USB streaming algorithms showed that a speed of up to 380 MB/s could be achieved (see Figure 4a and b). Timing constraints were derived from the initial benchmark specifying the maximum time for the FPGA to transmit a block of data before inserting dummy packets into the stream to stabilise the stream avoiding any re-connection or timeout of the USB protocol (see Figure 4c). Analysing the streaming parameters showed that larger transfers have the highest impact on the data rate while increasing the block size to values higher than 1 kB only showed minor improvements.

3.3 Reducing Image Blur from Detector Fluorescence

Imaging experiments with monochromatic X-rays can show blurring effects from fluorescence photons of the CdTe sensor spreading to other pixels. Utilising charge sharing together with simultaneous energy and timing information that TIMEPIX3 can provide, the fluorescence from

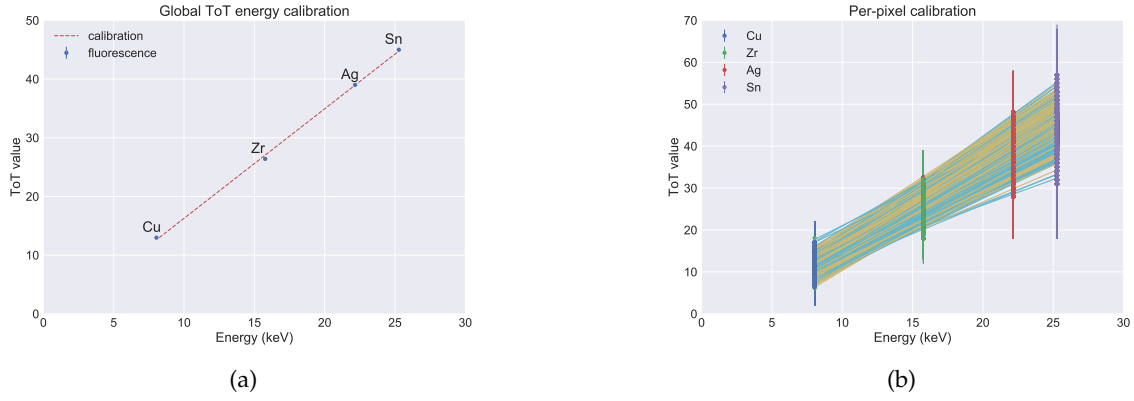


Figure 3: (a) Global energy calibration of the detector using fluorescence. (b) Per-pixel energy calibration using fluorescence with 4096 calibration curves plotted into the figure.

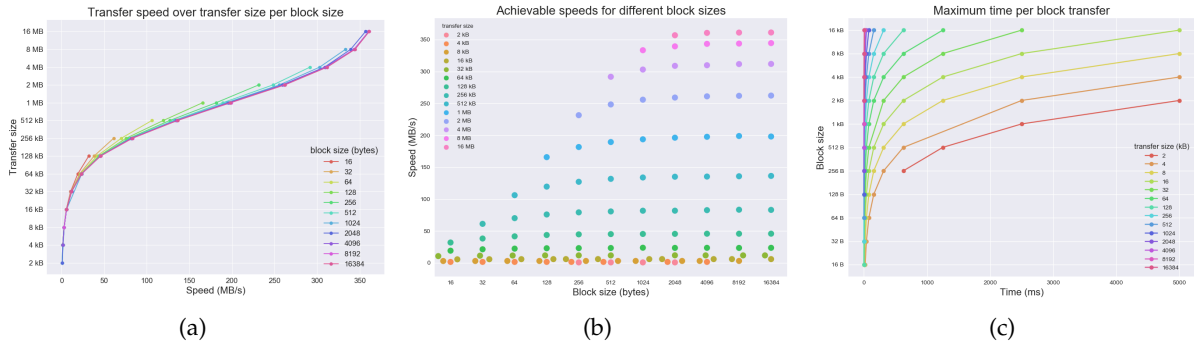


Figure 4: (a) Achieved data rates for different transfer sizes and block sizes. (b) Effect of different block sizes in combination with the transfer size onto the data rate. (c) Calculated maximum time the readout system has to provide one block of data or input dummy data into the stream.

the detector material can be conveyed to the pixel of origin. Changes in resolution can be quantified using the *modulation transfer function* (MTF) [14]. The MTF is the Fourier transform of the detector's *line spread function* (LSF), which can be derived from the *spatial frequency response* (SFR) and describes the attenuation of spatial frequencies by the detector response [15].

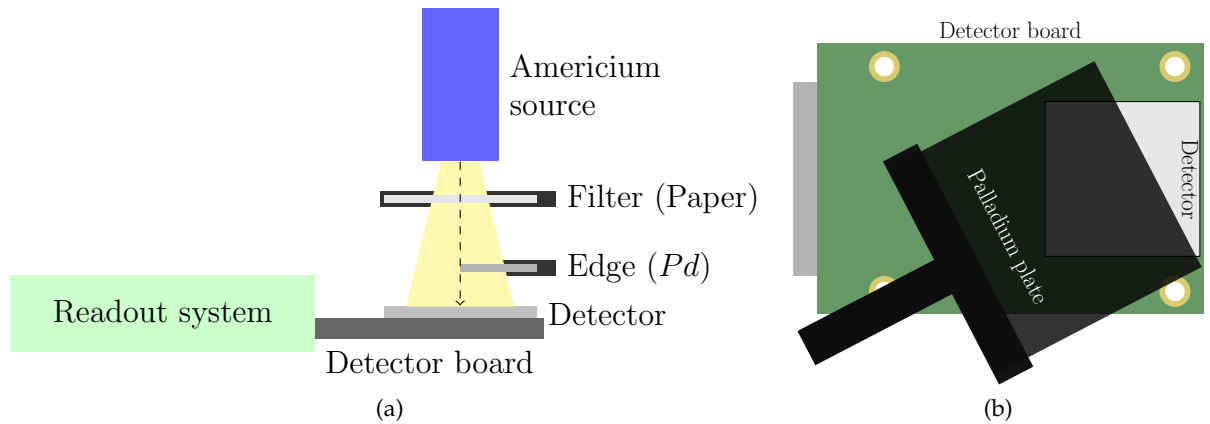


Figure 5: Setup used for edge measurement with a Palladium plate above the detector with the Am-241 source and a paper filter. (a) side view, (b) top view showing the slanted edge.

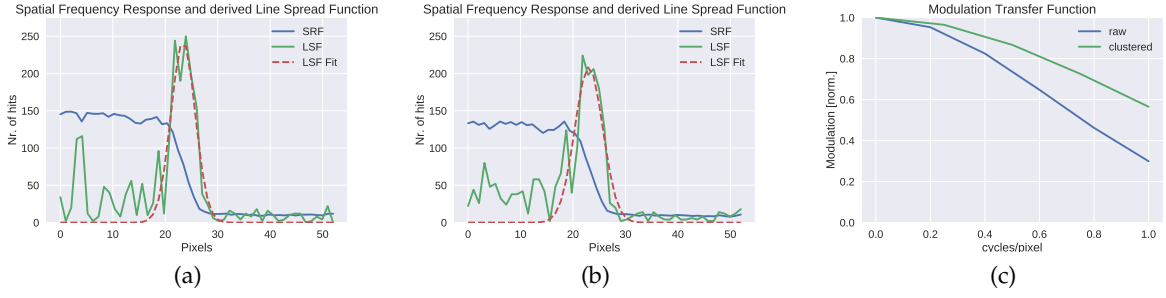


Figure 6: SPF response and LSF of (a) raw data and (b) clustered data. (c) MTF of both images showing an improved edge resolution for the processed data.

A standard approach to determine a detectors resolution is the slanted edge method [16], where part of the detector is covered with an object at a lower angle [17, 15]. As an edge, we used a 1 mm thick Palladium plate placed about 1 cm above the detector surface and slanted by ca. 14° towards pixel columns (see Figure 5). The 59.5 keV gamma line of a Americium-241 radiation source was used blocking alpha particles with a paper filter. The resulting data is scanned for clusters matching 59.5 keV. These clusters are then analysed for K_α or K_β peaks from Cadmium and Tellurium, 23.17 keV and 26.09 keV, or 27.27 keV and 30.99 keV respectively. These hits are identified unequivocally under low flux conditions by variations of the 1.56 ns *fast-Time-of-Arrival* (fToA) time stamp by ± 3 clock cycles with respect to the rest of the cluster. Identified fluorescence hits are added back into the cluster.

Analysing the images using the slanted edge approach described above shows an improvement of the resolution after clustering (see Figure 6c). The MTF shows a small improvement at half the Nyquist frequency, which signifies an improvement in detector resolution. Furthermore, the MTF does not converge towards 0, because the Palladium plate does not absorb 100% of the incoming radiation. The SFR and LSF of the clustered data (Figure 6b) look slightly clearer compared to the raw data (Figure 6a). The quality of those measurements is limited due to a high amount of defect pixels in the used CdTe detector.

4 Conclusion

A USB 3.0-based readout system for TIMEPIX3 hybrid pixel detectors was implemented. It uses standard USB communication and data streaming interface, which is implemented using an Opal Kelly development board consisting of an FPGA with an ARM co-processor managing the USB 3.0 interface. Data streaming is controlled via an algorithm managing the streaming parameters to archive a maximum speed of around 380 MB/s. This allows to maintain a hit rate of more than 40 MHit/s. The FPGA firmware has been designed with on-board processing in mind which will be important for future generations of the MEDIPIX and TIMEPIX ASICs that have a higher data rate. Furthermore, we demonstrated a way to improve the detector's resolution utilising the simultaneous energy and time information in combination with high-Z detector materials.

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