M.Sc. Thesis
In Electrical Engineering, 30 points

FPGA based smart NIR camera

Haoming Zeng
Abstract

Road conditions are a critical issue for road users as, if not given sufficient attention, they may threaten users’ lives. The environmental parameters, such as snowy, icy, dry and wet, are important in relation to the condition of roads. This is particularly true in relation to the northern regions and greatest concern should be in relation to snowy and icy situations. In this thesis, a system based on an InGaAs area scan sensor utilizes NIR technology to detect water or ice on the road so as to enable drivers to avoid slippery road conditions. The conditions caused by freezing water on road surface are particularly dangerous and are not easy to observe and it is hope that this project will boost traffic safety. The system is able to assist road maintenance personnel in forecasting and detecting slippery road conditions during winter road maintenance (WRM).

The system, which is based on FPGA, has functionalities that display the captured images on an HDMI monitor and send the images to the software on a host PC via the UART protocol. An interface board, which carries the sensor and which connects to the FPGA board, is developed for NIR sensor. VHDL implementation and PC software design are the works included in the project. Besides, this device is exploited utilizing InGaAs image sensor. According to its features, it can be applied in other applications which will also be discussed. Finally, experiments are conducted in order to investigate the system’s operation with the variation of temperature.

Keywords: Road condition, traffic safety, WRM, NIR, FPGA.
Acknowledgements / Foreword

First of all, I want to express my appreciation to my supervisor Benny Thörnberg for his patient guidance and intellectual support and many thanks to the colleagues at the Electronics Design Division for providing an excellent study environment for us.

I also want to thank Qing Liu, Xiaozhou Meng and Askan for their discussions and cooperation. Finally, I wish to express my appreciations to my parents, Wei Zeng and Lina Huang, for their trust and devotion. I am forever indebted to them.
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# Terminology / Notation

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</tr>
</thead>
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<tr>
<td>FPGA</td>
<td>Field-programmable gate array</td>
</tr>
<tr>
<td>NIR</td>
<td>Near infra red</td>
</tr>
<tr>
<td>RWiS</td>
<td>Road weather information system</td>
</tr>
<tr>
<td>WRM</td>
<td>Winter road maintenance</td>
</tr>
<tr>
<td>NIRS</td>
<td>Near Infrared spectroscopy</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>VHDL</td>
<td>Very-High-Speed Integrated Circuit Hardware Description Language</td>
</tr>
<tr>
<td>MCU</td>
<td>Memory control unit</td>
</tr>
<tr>
<td>HDMI</td>
<td>High-Definition Multimedia Interface</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver/Transmitter</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal Noise Ratio</td>
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1 Introduction

The report addresses an approach to developing an FPGA-based hardware framework integrating NIR sensor. The background of the project is in relation to the monitoring of winter road conditions. Additionally, according to NIR technology, the system is also able to be applied in other applications which will also be introduced. In this chapter, the background and the motivation behind the project will be presented. Furthermore an overall aim and the problems associated with the project are stated. An outline of the thesis will also be given at the end of this chapter.

1.1 Background and problem motivation

Road traffic safety always draws people’s attention, since road traffic forms major part in the daily lives of many people and thus is directly related to them. In order to improve road traffic safety, the detection of the road condition has now become a crucial issue. It is essential that official departments do take necessary measures to ensure safety as far as possible. Road weather information system (RWiS) is one of the world’s most widely implemented weather information services for road traffic [1], providing information, such as radar and satellite images, which is given in real time to WRM personnel. The Swedish RWiS has more than 600 roadside stations equipped with sensors, which are able to measure several metrological variables [2]. The UK spends £482 million on the primary road network, while £1069 million is the cost involved for winter maintenance of local roads [3]. Based on a study of many cases, it is obviously that it is essential to have timely knowledge of road condition.

Over the years, based on the inventions and applications relating to high level technology and the maintenance personnel’s action, road traffic safety has been improved and the traffic accident rate has been reduced in many countries [3]. However, the problem do still exists.

There are many factors which can lead to traffic accidents, such as sudden illness, drink driving etc. The slipperiness of the road is one of the most dangerous situations, especially in northern regions such as Sweden, Finland etc. where the low temperature can easily cause slipery
For example, in Finland, about 25% of all fatal accidents occur on icy and snowy road surfaces [2]. Additionally, in Edmonton, Canada, 40% of the traffic accidents occur due to ice/snow or rain covering road [3]. It is thus extremely important that the maintenance personnel pay sufficient attention and perform suitable and timely actions on the WRM. It is also necessary to inform the road users of abnormal road situations in order to reduce the risk of traffic accidents.

The serious problem caused by the slipperiness of the road is always the result of the formation of icy patches which will readily occurred after rain or snow on a frosty road. It is caused by an objective factor, which can be avoided, if sufficient measures are taken. However, a bad situation is faced that when the ice on road is thin and thus may be difficult to observe but which is extremely dangerous. Under these conditions, highly accurate and highly efficiency methods are always required. Knowledge relating to the road surface temperature provides important information with regards to an ice slipperiness warning system. Hence, in this paper, a system based on NIR technology is proposed in order to solve this problem and an evaluation of it will also be made.

Historically, in 1800, Herschel used a prism to separate the electromagnetic spectrum and thus was able to discover the NIR region. In the early 1920s, many NIR experiments were carried out, but it was not widely applied until the mid 1960s. The potential of the NIR technique was realized by Karl Norris and he used technique in an industrial field under the name “Morden NIRS”. The reason why the NIR technology was utilized based on its important features. Infrared light has a longer wavelength than visible light and its wavelength corresponds to a frequency range approximately 1 to 400 THz, and includes most of thermal radiation emitted by objects [4]. Based on the principle, the system is able to manage the monitoring of the road surface.

NIRS (Near Infrared spectroscopy) is a method based on molecular overtone and combination vibrations. The absorption bands are prominent in NIR region in relation to the -CH, -NH, -OH, -SH functional group. NIRS technique covers both the wavelength range adjacent to the mid infrared and the visible region. Based on this technique, the proposed system can provide a sense of the situation relating to ice and water.
NIR has also been applied practically in areas, including agriculture, remote monitoring, medical uses, material science etc [5].

In terms of the platform and based on the rapid development of silicon technology, FPGA has been chosen due to its high performance and high capacity features which make it suitable for a complex hardware design such as image processing.

1.2 Overall aim
This thesis project’s overall aim is to develop a primary hardware framework for an NIR camera in relation to capturing, storing and displaying images. In addition, an analysis of the images will also be evaluated.

According to the proposal, the overall aim is divided into four parts to show more detail.

- Develop an interface PCB board for NIR image sensor
- VHDL implementation for display and communication with PC
- Software design on PC for storage
- Analyse the generated images by NIR sensor

1.3 Problem statement
In this thesis project, during the design of the interface board, the problems associated with the type of required circuit are studied. The solution for this includes a high speed amplifier, high speed AD conversion circuit and 5V and 3.3V logic level conversion circuits. In addition, a compatible connector for ATLYS FPGA board should be carried, which has an influence on the thickness and shape of the PCB board.

In terms of VHDL implementation, the problems arise from the control of the NIR sensor and the pixels generation, communication with the PC via the UART protocol, and the display of the images on an HDMI monitor. During the programming, the delay of the AD conversion should also be considered.

In software design, the problems that send the command to FPGA and receive data and save the image as a BMP file should be solved. A
highly robust system, friendly GUI and low error rate of receiving data are required for the software thus requiring many tests.

After the hardware structure has been designed and the PCB manufactured, the soldering components onto the PCB also requires a strategy to be adopted in order to ensure that each part works in a satisfactory manner. Finally, an investigation is processed to evaluate the images’ quality under a variation in temperature.

1.4 Contribution
The FPGA platform operates with functions for monitor displaying and a mechanism for frame buffering, which are provided by my supervisor Benny Thörnberg. The function of UART communication has been performed by Ashkan Hashemi, while the function of the sensor readout and some modifications to the UART communication are conducted by the author of this report.

The VB software and PCB are also designed by the author. Some of the circuits for the PCB design have been provided by the author’s supervisor. Additionally, the assembling of device has been performed with assistance from author’s supervisor.

1.5 Outline
Chapter 2 states the related work of the project;

Chapter 3 provides a model for the system. Additionally, the PCB, FPGA implementation and software’s architecture will be illustrated.

Chapter 4 elaborates the procedures during the implementation and provides the detail of the design.

The result is presented in Chapter 5 and a conclusion/discussion is given in Chapter 6.
2 Related work

Many methods have been exploited in recent years for road traffic safety. For northern regions, the slipperiness of road problem is the outstanding problem and a mounted sensor is one approach to studying it. It is possible to forecast the frost on the road surface which may lead to it becoming slippery [6].

Furthermore, there is a comparison between a passive and active sensor made by Patrik Jonsson for road detection consideration [7]. He also conducted research combining meteorological sensors and camera images from RWiS in order to improve the road condition classification [8]. Methods such as neural networks [8], Support Vector Machines (SVM) [9], multivariate analysis [10] and etc are also studied.

All objects emit energies called thermal radiation due to its temperature and IR is sensitive to this. Based on this feature, many applications have been developed such as night vision devices, thermal imaging, communications and etc [11].

According to the research, IR has a higher reliability than mounted sensors when applied to surface temperature reading during wet, snowy or icy road conditions [12]. Additionally, NIR is one kind of IR with 0.75um to 1.4um wavelength. NIR technology has been used in freezing point detection in some cases [13]. Thus the NIR technology is dedicate to this project’s development.
3 Methodology

The purpose of the system is elaborated in the previous chapter and thus the architecture of the whole system will be described.

The whole system basic operation flow chart is shown as Figure 3-1:

![Flow Chart](image)

**Figure 3-1 Abstract of system architecture**

1) Image capture: NIR sensor is planned to be applied for image capturing. It is necessary to design a PCB board to read out the data from the sensor.

2) Image processing: This step is realized in the FPGA board for which ATLYS is chosen. Displaying the images on an HDMI interface monitor is an essential part in order to study the result. It also operates to send image data to a host PC via UART protocol. This process will be implemented in the FPGA board.

3) Further processing: Finally, it is able to restore, save and display the image after receiving data from the second step. Hence the image can be used for analysis, for instance, by using MATLAB. The functions will be realized by means of the software on a PC.

After analysing the functions of each part, the architecture can be defined as the diagram Figure 3-2 and the stereogram Figure 3-3.
3.1.1 Architecture of PCB
As stated in the previous description, a PCB will be designed so that it can carry the NIR sensor and connect it to the FPGA board. After studying the sensor, which is also introduced in next chapter, the work flow of the PCB is as shown in Figure 3- 4.
3.1.2 Architecture of FPGA implementation

VHDL is the language used for the FPGA implementation. The functions for this part are to receive the data from the sensor, generate pixel data and a timing sequence, display the captured images on monitor with an HDMI interface, and communicate with a host PC via USB. Accordingly, the general architecture of FPGA system is as shown in Figure 3- 5.

3.1.3 Architecture of software

The software is used for receiving data and saving them into a file on the PC.

Some demands were required after due consideration. Firstly, GUI is necessary for the user’s convenience. The port and bound rate is selectable in the interface. Other functions such as displaying the received
value, sending a command by clicking a button are the improvements which have been in the GUI design. Because image processing involves such a large quantity and a high speed process, the software ought to be highly reliable when working at a high speed. In relation to storage, the BMP file is chosen because of its uncompressing feature.

The basic work flow is shown in Figure 3-6.

![Figure 3-6 Software architecture](image)

### 3.1.4 Experimental evaluation

Finally, an evaluation should be conducted in order to evaluate the system. The experiments are based on the deployment of the equipments as shown in the Figure 3-7. The white colour reflects the Infra Red light, while the black colour absorbs it.

![Figure 3-7 Deployment of equipments](image)
It is thus able to capture an image for which half is white and the other half black. The region A, obtained from the white part, is the foreground and B, obtained from black part, is background. After the calculations by means of the formula below, the SNR of images can be known. The calculation will be conducted by using MATLAB.

\[
\text{SNR} = \frac{\text{meanA} - \text{meanB}}{\text{stdA}}
\]

**Formula- 1 SNR calculation**

According to the feather of the NIR detector, it integrates a one stage cooler, which is able to control the detector’s temperature and a thermistor by which the temperature is known after measurements are taken according to Figure 4-3. Hence, it is possible to study the variations of the SNR with the changing of the sensor’s temperature.

Additionally, after compilation by means of an ISE tool, a report will be generated which provides the information of FPGA usage, including the used LUTs and the slices and block RAMs. The Xpower Analyzer, which is integrated in the ISE tool and is a tool for the power analysis of routed or post-implemented designs, is used. The Digilent Adept software contains the function of measuring the power consumption in real time. These three tools will provide more details in relation to the system.
4 Design / Implementation

This chapter focuses on the implementation of the system including schematic and layout design for the PCB, soldering components onto PCB, the assembling of the device, the FPGA implementation and the software design. However, before this, an introduction of the hardware components is essential for further understanding.

4.1 Hardware introduction

4.1.1 NIR sensor

The NIR sensor comes from a Japanese company Hamamastu. The picture below is the sensor. The sensor is hermetically sealed in TO-8 package together with a one stage thermoelectric cooler which make it into a highly stable operation [14]. The features of this sensor also include the 0.95 to 1.7μm range of spectral response, excellent linearity, high sensitivity and a built-in timing generator.

![NIR sensor](image)

Figure 4-1 NIR sensor [14]

It is an area image sensor utilizing an InGaAs photodiode. A CMOS readout circuit is integrated as shown in Figure 4-2. The signal processing circuit will hold the optical information as signal voltage. Then the amplifier will be reset in each pixel and the reset voltage will be transferred to the signal processing circuit. Thus the voltage difference between the optical information voltage signal and the reset signal can be calculated by means of the offset compensation circuit. The shift register works to scan the data storing in the signal processing circuit.
from right to left. The image sensor is able to generate 64 by 64 pixels’
two dimensional infrared imaging. Each pixel size is 50*50 um and the
image size is 3.2*3.2mm. Thus an optical lens is required to in order to
obtain a wider visual field.

The sensor can also be applied in many applications, for instance, ther-
mal imaging monitor, laser beam profiler and near infrared image
detection which are listed in its datasheet.

Because a one stage cooler is integrated in the image sensor, an evalua-
tion will take advantage of it in order to investigate the operation of the
system under various temperature conditions.

According to the purpose of the project, the system may work in ex-
treme environments. The cooler is able to control the sensor’s tempera-
ture during the operation of the system so as to ensure the quality of the
results. Hence, from the experiments, it is important to study the impact
of the cooler. In the datasheet, three diagrams are given as follows in
order to illustrate how to select the input power source.
According to Figure 4-3, Figure 4-4 and Figure 4-5, it can be seen that a constant voltage power source can be given in order to adjust the temperatur-
perature of the sensor. The temperature can be measured through the changes of the thermistor resistance according to Figure 4-6. In addition, the constraints of the cooler input are given to protect the sensor from being destroyed.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE-cooler allowable current</td>
<td>Ic</td>
<td>-</td>
<td>0.7</td>
<td>1.1</td>
<td>A</td>
</tr>
<tr>
<td>TE-cooler allowable voltage</td>
<td>Vc</td>
<td>-</td>
<td>1.0</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>Thermistor resistance</td>
<td>Rth</td>
<td>8.8</td>
<td>9</td>
<td>9.2</td>
<td>kΩ</td>
</tr>
<tr>
<td>Thermistor power dissipation</td>
<td>Pth</td>
<td>-</td>
<td>-</td>
<td>0.2</td>
<td>mW</td>
</tr>
</tbody>
</table>

Figure 4-6 Specifications of TE-cooler

4.1.2 ATLYS FPGA board

The FPGA board chosen is the ATLYS from Digilent Inc. The ALTYS circuit board is a ready-to-use development platform based on a Xilinx Spartan6 LX45 FPGA in a 324-pin BGA package. The Spartan6 LX45 is an optimized choice for high performance consideration with 6822 slices and a 500MHz clock speed.

Furthermore, Figure 4-8 shows the detailed components on the board. The platform includes an HDMI port, USB-UART and DDR2 memory which will be used in the project.
The power supply is an essential part of the board. It requires an external 5V power source. Voltage regulator circuits from Linear Technology create the required 3.3V, 2.5V, 1.8V, 1.0V, and 0.9V supplies from the main 5V supply. Table 4-1 provides the information with regards to each circuit working with the relevant voltage.

<table>
<thead>
<tr>
<th>Supply</th>
<th>Circuits</th>
<th>Device</th>
<th>Amps (max/typ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>FPGA I/O, video, USB ports, clocks, ROM, audio</td>
<td>LT3501</td>
<td>3A / 900mA</td>
</tr>
<tr>
<td>2.5V</td>
<td>FPGA aux, VHDC, Ethernet PHY I/O, GPIO</td>
<td>LT3546</td>
<td>1A / 400mA</td>
</tr>
<tr>
<td>1.2V</td>
<td>FPGA core, Ethernet PHY core</td>
<td>LT3546</td>
<td>3A / 0.8 – 1.8A</td>
</tr>
<tr>
<td>1.8V</td>
<td>DDR &amp; FPGA DDR I/O</td>
<td>LT3501</td>
<td>3A / 0.5 – 1.2A</td>
</tr>
<tr>
<td>0.9V</td>
<td>DDR termination voltage (V+)</td>
<td>LT3413</td>
<td>3A / 900mA</td>
</tr>
</tbody>
</table>

As shown in the table, the FPGA I/O works with 3.3V power and some GPIOs use 2.5V, which would suggest that the logical level is merely 3.3V or 2.5V. This would be a challenge in the future schematic design since the NIR sensor and ADS803 operating at 5V logic. The solution with regards of this issue will be addressed in the next section.

In addition, the DDR2 memory on board is used for the frame buffer of the FPGA implementation which is controlled by the memory control unit. The ATLYS board also contains four HDMI ports, including two buffered HDMI input/output ports, one buffer HDMI output port, and one without buffering that can be input and output. As for the commu-
In order to connect the FPGA platform and the NIR camera, the expansion connector must be studied in order to design an interface with the PCB. Figure 4- 9 shows the connector’s general view. The black dots are connected to the ground.

![Figure 4-9 VHDC connector](image)

### 4.2 PCB design

#### 4.2.1 Schematic design

Based on the information previously introduced, first of all, the schematic should be designed for this PCB board in order to provide an interface between the sensor and the FPGA board. In the previous chapter, the survey of the design has been discussed. The schematic for each part will be illustrated in the following section.

The NIR sensor’s library is designed shown in Figure 4- 10 which also shows the pins. The right one is the package of the sensor.

![Figure 4-10 NIR Sensor Library](image)
As shown in Figure 4-10, MSP is the signal for starting a new frame and for determining the exposure time. The AD_TROG indication of the output voltage is the pixel value. MCLK is the working clock with a maximal 40MHz. PD_bias requires a 4.5V power source. The circuit shown in Figure 4-11 is able to achieve this value by adjusting the potential meter.

![Figure 4-11 Circuit for 4.5V power generator](image)

VIDEO is the output signal which is presented as an analog signal and which indicates the pixel values. Due to the high speed operation of the system, a high speed ADC is required. Additionally, according to the datasheet, a voltage follower is necessary in order to enhance the VIDEO signal operation. The MAX452 is selected which is a 50HZ video amplifier.

The AD converter is the heart of this board. ADS803 is chosen, because of its high speed, high dynamic range, 12 bit pipelined and maximal 5MHz sampling features. The circuit of ADC is the same as that for Figure 4-12.

![Figure 4-12 ADS803 converter circuit](image)

It is necessary to illustrate the detail for this AD converter. Firstly, its detected range is able to be determined by using the circuit as shown in Figure 4-13.
The figure is obtained from its datasheet [15], the computational formula is also in the figure. Accordingly, with an inverse input connecting to 2.5V, the range of measuring is from 1V to 4V as shown in the figure. The VIDEO output voltage, according to datasheet, is from 1.2V to 3.2V which falls within the range.

Another consideration relates to how to generate 2.5V to -IN. In the ADC, it is possible to produce this by taking advantage of the top and bottom references associated with a simple circuit. Figure 4-14 shows the circuit.

The top reference provides a +3V source, and the bottom one provides +2V. Only two 2KΩ resistors are used.

In consideration to the power source for IC, -5V is required by MAX452 and LM741. The -5V generation circuit is the same as for Figure 4-15.
After implementation of the above circuit, the decision was that the MAX660 should replace ICL7660 which has a higher drop voltage.

A challenge is coming when studying the FPGA board. As mentioned in the previous section, FPGA I/O works with 3.3V logic. However, ADC and the NIR sensor require 5V logic level. Thus the logic conversion is essential.

Table 4-2 FPGA I/O standard and levels [16]

Table 4-2 is the list showing the I/O standard of ATLYS and its logic levels. The LVCMOS33 I/O standard is planned to be implemented in The FPGA I/O communication with the PCB. FPGA must generate a clock signal to the NIR sensor and the ADC. Therefore, a means of converting the 3.3V to 5V logic IC is required. After searching, Table 4-3 and Table 4-4, the characters of 74HC32 and 74HCT32 family chips from their datasheet, are 2 inputs or gates that may be applied in relation to this conversion.
The two tables state their electrical characteristics. It is necessary to study it in order to ensure make sure the robust operation of the design. Comparing two tables, in order to illustrate which family is suitable for the project, a figure is drawn as shown below.

![Figure 4-16 Digital level characters](image_url)
From the figure above, it shows that when determining the low level both 74HC and 74HCT works in a satisfactory manner. However, in relation to high level judgment, only the 74HCT is able to guarantee the correct operation. For an example, if the FPGA I/O provides a 2.4V high logic, then 74HCT is able to classify it to a high logic input while the 74HC is unable to. So the 74HCT32 is chosen for 3.3V to 5V logic conversion. In addition, the NIR sensor will output an AD trigger signal (5V logic) to FPAG. For this reason, the 74HC4050 is accordingly chosen in the project by using same principle. The output logic level of the ADS803 can be easily selected by connecting a 3.3V power to the output driver pin.

The appearance of the system is also an important point to be considered. A metal basement is required to ensure temperature uniformity of the NIR sensor.

Figure 4-17 shows the system’s appearance. In this regard, the PCB should have two parts, which are named as the “PCB female board” and the “PCB male board”. The connectors are used to connect the female board and the male board, the FPGA platform and the male board as shown in the figure. The library of connector, such as VHDCP, is provided as the following schematics.
As seen in Figure 4-18 and Figure 4-19, there are plenty of decoupling capacitors connecting between the power source (5V, 3.3V and -5V) and the ground in order to reduce the noise.

**4.2.2 PCB layout**

After designing the schematic, the components are exported to the PCB design. Rooting wires is the next task and there are some important points in relation to this. As the previous description, two parts will be put into one PCB and they will be separated by holes as shown in the Figure 4-20. A four layers design proposal is applied since not only the
ground and power wired will be simpler, but, it will also increase the quality of the signal processing. The layers are shown in the figure.

During the wiring, the width of the ground and the power wire should be wider. The location of the decoupling capacitors, which are deployed close to the power input of each IC components, must be carefully chosen.

In addition, according to the application, the requirement is that the components are to be deployed in the top side, which assists in assembly of the system with regards to the appearance of the device. The holes along the border are designed for mechanical stability. The text such as “C16”, “74HCT32” ought to avoid covering the pads and it remain visible after the soldering of the components. In addition, the analog part, such as the 4.5V and -5V generating circuit, should not be close to the digital part, such as the ADC circuit, with the aim of avoiding any disturbance between them. The next figure displays the domains of the different power sources.
When designing the PCB boundary, as seen in Figure 4-23, the red circle part, which plugs into VHDCP connector, is an essential consideration.
Studying the specification of the VHDCI connector, the requirement is for the board thickness to be 0.80mm and the length of the connect head to be 28.20mm. Accordingly, the dimensions of the PCB are specified as shown in Figure 4-24.

![Figure 4-24 PCB outline dimension](image)

Some more detailed information is provided when the design is send for manufacture in order to ensure a high quality product.

1. Total board thickness: 0.8 mm
2. Minimum clearance copper to copper: 8 mil
3. Minimum copper track width: 8 mil
4. Copper thickness for Layer1 and Layer 4: min 18 um

5. Copper thickness for Layer2 and Layer 3: min 35 um

6. Material: FR4


Furthermore, the files listed in Table 4-5 are required by the factory.

<table>
<thead>
<tr>
<th>File extension</th>
<th>Used for</th>
<th>Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>.cmp</td>
<td>Copper tracks, Vias, Pads</td>
<td>Layer 1, Component side</td>
</tr>
<tr>
<td>.ly2</td>
<td>Ground plane, Vias, Pads</td>
<td>Layer2</td>
</tr>
<tr>
<td>.ly3</td>
<td>Power supply plane, Vias, Pads</td>
<td>Layer3</td>
</tr>
<tr>
<td>.sol</td>
<td>Copper tracks, Vias, Pads</td>
<td>Layer 4, Solder side</td>
</tr>
<tr>
<td>.plc</td>
<td>Printing</td>
<td>Silkscreen on component side</td>
</tr>
<tr>
<td>.pls</td>
<td>Printing</td>
<td>Silkscreen on solder side</td>
</tr>
<tr>
<td>.stc</td>
<td>Solder stop mask</td>
<td>Solder stop mask on component side</td>
</tr>
<tr>
<td>.sts</td>
<td>Solder stop mask</td>
<td>Solder stop mask on solder side</td>
</tr>
<tr>
<td>.drd</td>
<td>Drills, Holes</td>
<td>Drill data</td>
</tr>
<tr>
<td>.lyx</td>
<td>Cutting of board edges</td>
<td>Physical board outline drawing</td>
</tr>
</tbody>
</table>

Table 4-5 Required files and its specification

Figure 4-25 shows the actual appearance after manufacturing.
4.2.3 PCB circuits testing and soldering

Before installing the NIR sensor, the strategy for soldering and testing in relation to the consistency of the operation of the PCB circuits falling in line with the expectations is made as follows. The steps are in same order as for the experiment.

Step 1: Male board testing; Firstly, the male board should be soldered and ensure that the ground and VCC are separated. Then the I/Os’ signal should be in the correct order.

Step 2: -5 power source testing; -5V power is necessary for amplifier and the 4.5V generator circuit.

Step 3: 4.5V generator testing;

Step 4: Logic level converter; the logic signals are generated from the FPGA.

Step 5: Voltage follower; using square signals to check the response time of the amplifier and observing the noise of the output.

Step 6: AD converter testing; an external adjustable DC power source is employed and the readout data are sent to the PC via the UART
4.2.4 Device assembling

The mechanical structure is quite important in this project. Based on the overview of the device presented in the previous section, a metal base as shown in Figure 4-26 is required.

![Figure 4-26 Metal base of device](image)

Hence, the drilling of the holes is next the step before the assembling can take place. According to the dimension of the sensor, the holes’ diameters are marked in the figure.

![Figure 4-27 NIR sensor dimension](image)

As Figure 4-28 shows, the diameter of the hole for the sensor is 14mm. Additionally, the four holes classified as hold A ought to be drilled to correspond with the PCB design, which is 3.5mm, in order to fix the PCB board. In order to drilling these holes, a 2.5mm drill is firstly used, after which a tool to drill the thread is used. Hold B is used to fix the optical lens. The two holds are 2mm. With the same principle as for hold A drilling, hold B is drilled using 1.5mm after which the threads are drilled. In order to achieve a large range of vision, an optical lens is integrated.
covering the sensor. The holes for fixing the lens must also be drilled on the vertical board as shown in the figure.

Figure 4-28 Holds on vertical metal board

The end product is as follows:

Figure 4-29 End product of project
4.3 VHDL implementation

The FPGA handles the image data from the sensor for displaying and sending to the PC. As for the previous description of the VHDL implementation architecture, this part contains the NIR controller, Frame Buffer, DDR signal processing, HDMI signal processing and UART signal processing.

4.3.1 NIR controller implementation

The NIR controller outputs the clock signal, start signal to the NIR sensor and the clock signal to the AD converter. The AD converter generates 12 bits of data to the controller. Figure 4-30 is the timing chart of the sensor. Figure 4-31 is the AD converter’s time diagram.

![Figure 4-30 Timing chart of NIR sensor](image1)

![Figure 4-31 Timing diagram of ADS803](image2)

After a new frame is started, which is triggered by MSP signal, a 90 MCLK blank period will follow. Then the NIR sensor will output the AD trigger signal within the period of the 8 MCLK. When the AD trigger’s signal is coming, the AD converter will generate the corresponding data after 6 clock cycles of the AD. The step is named as “wait data available”. According to this mechanism, the work flow is designed.
The entity is established as shown below. The pixels data, fsync and rsync are generated and transferred to the MCU (memory control unit). The bits of “Data out” are compressed from the AD output data which is 12 bits to 8 bits, so as to be compatible with the UART processing.

![Diagram](https://via.placeholder.com/150)

**Figure 4-32 Work flow of NIR controller**

The reset period is 200 MCLK, the blank between each line is 94 MCLK and the integration is time 40MCLK, which is provided in datasheet, should also be considered.

Additionally, the output of the ADC is 12bits while the data bit width of the UART is 8bits. Thus, based on the principle, the 1.2V corresponds to 0 in the pixel value, and the 3.2V to 255. A calculation, both for downscaling from 12bits to 8bits and adjusting the zero level from 1V to
1.2V, is thus required. The formula is constructed in order to manage this and is also applied in the VHDL project.

Equation (1): \( \text{Din} \times (\text{REFT}-\text{REFB})/2^{12} = \text{Vadc} - 1V \)

Equation (2): \( \text{Dout} \times (\text{VDmax}-\text{VDmin})/2^{8} = \text{Vadc} - \text{VDmin} \)

According to Equation 1 and 2, the formula is calculated as Formula 1.

Equation (3): \( \text{Dout} = \text{Din} \times 3/32 - 25.6 \)

**Formula- 2 Downscaling calculation**

In the application, the REFT is 4V, and the REFB is 1V. Vadc is the output voltage of the AD converter. VDmax is the maximum value of the sensor’s output while VDmin is the minimum value. Din is the integer value after conversion from the 12 bits value by the VHDL function. Dout is converted to the 8bits value finally as the output for the UART controller.

### 4.3.2 Frame Buffer

The frame buffer receives data from the NIR controller and stores them into the DDR. And the HDMI and the UART controller will read out the frame data out. These controlling processes are realized by the MCU.

As shown in the Figure 4-34, the MCU has 3 ports. Port A reads data from the NIR controller. Port B writes data into the DDR and reads them out. Port C sends data to the UART or the HDMI which is chosen by the Memory Control Unit.
PC command. If the PC sends data to the FPGA, the data will be sent out to the PC via the UART. At the same time, the monitor will be turned off. After a whole frame has been transferred to the PC, the frame will be stored as a BMP file without compression, and the monitor will work again. This module is designed by Digilent.

4.3.3 HDMI controller

The communication with the monitor is based on an HDMI cable. The HDMI interface outlook is as shown in Figure 4-35. The figure also includes the Pin function.

![HDMI interface](image)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TMDS Data2+</td>
</tr>
<tr>
<td>2</td>
<td>TMDS Data2 Shield</td>
</tr>
<tr>
<td>3</td>
<td>TMDS Data2-</td>
</tr>
<tr>
<td>4</td>
<td>TMDS Data1+</td>
</tr>
<tr>
<td>5</td>
<td>TMDS Data1 Shield</td>
</tr>
<tr>
<td>6</td>
<td>TMDS Data1-</td>
</tr>
<tr>
<td>7</td>
<td>TMDS Data0+</td>
</tr>
<tr>
<td>8</td>
<td>TMDS Data0 Shield</td>
</tr>
<tr>
<td>9</td>
<td>TMDS Data0-</td>
</tr>
<tr>
<td>10</td>
<td>TMDS Clock+</td>
</tr>
<tr>
<td>11</td>
<td>TMDS Clock Shield</td>
</tr>
<tr>
<td>12</td>
<td>TMDS Clock-</td>
</tr>
<tr>
<td>13</td>
<td>CEC</td>
</tr>
<tr>
<td>14</td>
<td>Reserved (HDMI 1.0-1.3c),</td>
</tr>
<tr>
<td></td>
<td>NEC Data- (Optional, HDMI</td>
</tr>
<tr>
<td></td>
<td>1.4+ with Ethernet)</td>
</tr>
<tr>
<td>15</td>
<td>SCL (I2C Serial Clock for DDC)</td>
</tr>
<tr>
<td>16</td>
<td>SDA (I2C Serial Data Line for DDC)</td>
</tr>
<tr>
<td>17</td>
<td>DDC/CEC/HEC Ground</td>
</tr>
<tr>
<td>18</td>
<td>+5 V (max 50 mA)</td>
</tr>
<tr>
<td>19</td>
<td>Hot Plug detect (all versions) and NEC Data+ (optional, HDMI 1.4+ with Ethernet)</td>
</tr>
</tbody>
</table>

**Figure 4-35 HDMI interface**

HDMI is compatible with the DVI signals electrically. In the VHDL implementation, the DVI protocol is utilized. The entity is designed by Digilent as shown in Figure 4-36.
4.3.4 UART controller

The UART controller is in charge of the communication with the PC. When the PC sends a command to the FPGA, the image data will be read from the Frame Buffer and sent to the PC by means of the UART controller. The entity of the UART controller is as shown in Figure 4-37.

The UART will set the PC_COMMAND to ‘1’ after receiving command from the PC. The PC_COMMAND gives the command to the system to disconnect the monitor, reset the Frame Buffer address pointer and connect the Frame Buffer to the UART controller.
4.4 PC Software design

PC Software is required to save the images for further analysis. The data received from the FPGA is 8 bits per pixel. A BMP format without compression is chosen. The software is designed based on Visual Basic.

4.4.1 Graphic User Interface

As the Figure 4-38 shown, the image size can be predefined by through filling the value in the text box. Before the start, the COM port and baud rate must be selected. Then clicking the “Start” button can start the software. “Capture” is for capturing an image from the FPGA. By clicking the button, the software will send a command to the FPGA. Then the pixel data received will be plotted on a picture box on the left. After the pixel data fully fills the picture box, the image will be saved in the C disk automatically with the name of “NIR”. Alternatively, the “SAVE” button can save the image manually and clear the picture box.
The Figure 4-39 is the GUI when the software is on running. The picture box is rescaled according to the values in the text box. “Start” is invisible and “Reset” appears after the start. It is able to redefine the picture size, COM port and baud rate after clicking the “Reset” button. The state information is displayed on the right top.

4.4.2 Software Programming

The programming is based on Visual Basic which the UART protocol communication supports. The main procedure is UART communication. There are two ways to listen and process the received data.

The first one is by using a UART interrupter. Each time when the receiving buffer is full, it will interrupt the software to deal with the UART interrupt event. However, during processing including plotting on the picture box and writing data on the text box, the software will stop listening to the data from the UART which leads to data loss, while the second method overcomes the shortcut.

The second approach takes advantage of a timer. The mechanism is operating as follows. Each 0.5 second, the timer will interrupt the software to process the buffer data. During this time, the buffer still can receive the data. The buffer size is set to 20000 bytes which depends on the interrupter time. This method is implemented in the project.
Figure 4-40 Basic work flow of software
5 Results

This chapter will provide experimental results as well as an evaluation of the system performance based on different detector temperatures.

5.1 Experiment result

5.1.1 Placement and equipments
The common result is given from the deployment as in Figure 5-1.

![Figure 5-1 Placement of equipments](image)

The situation for this experiment is in relation to the situation of dark place. Based on the limitation of the equipments, a lamp, as shown in the figure shown is selected as NIR illuminator. The lamp uses a 50 Hz AC power source which leads to unstable results.

5.1.2 Result of monitor display
The monitor displays the black white video, the background of which is gray as in Figure 5-2. The 64 by 64 pixels image is shown on the left of the top.
5.1.3 Result of PC software

In the software, the width, the height of image, the COM port and baud rate are configured as in Figure 5-3. Then the “Capture” is active in order to capture the image from the software. In addition, the values of the pixel data are displayed in the text box on the right side.

5.1.4 Resource usage of FPGA

The report of the FPGA usage is derived from ISE tool, including information regarding used LUTs, slices and block RAMs.
5.1.5 Estimation of Power Consumption

For a hardware system, the power consumption is always an important factor. There are two approaches which are explored in order to estimate the power consumption of the FPGA design, not including that for the PCB.

Firstly, the Xpower Analyzer which is a tool for the power analysis of routed or post-implemented designs is used. The report is as follows under the condition of 25°C.
The Digilent Adept software contains the function of measuring power consumption in real time. The Figure 5-6 is the consumption estimation presented by the software.

As the figures shown, the estimation does not include the +5V power consumption. The first method only considers the consumption of VHDL design. However, measurement in the second method includes the 3.3V supply for the IC components on the PCB, for example, ADS803 and 74HC4050 while the first method does not.

5.2 Evaluation

This section elaborates the variation of the SNR images under different temperature conditions, which are created by using a TE-cooler integrated in the sensor. A voltage power supply was used as the TE-cooler’s input. According to the input constraints, the range of input voltage is from 0V to 1.5V. The input voltage was changed and the resistance of the thermal resistor in each sample was measured in order to obtain the chip temperature according to Figure 4-3. There are twelve
samples captured to analyze the variation of the SNR of the images as the temperature changing.

In order to achieve high quality results, numerous measures have been taken in order to reduce noise or disturbance as much as possible. The experiments were conducted at night which can avoid the disturbance from solar light, and the room lights are also turned off. Additionally, a flashlight is used as the illuminator, because the flashlight uses DC power which is better than the lamp using 50HZ AC. Although the power consumed by the flashlight is rather pretty high and the experiments will thus take a longer time, for the sake of maintaining the uniform of illumination, a constant DC power source is applied instead of the battery. Figure 5-7 is the experimental set up.

Figure 5-7 The placement of equipments

The black colour can absorb the NIR, while the white can reflect it. After the arrangement of the equipments, the images are captured as shown in Figure 5-8.
The size of the captured image is 64*64 pixels. In order to calculate SNR of the images, the area A is located as signal information, while B is the background. The Matlab file SNR.m is programmed to calculate the SNR. The results are shown in the Table 5-1.

<table>
<thead>
<tr>
<th>Temperature(℃)</th>
<th>23</th>
<th>20</th>
<th>17.500</th>
<th>13</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>meanA(ADC units)</td>
<td>243.4959</td>
<td>243.5372</td>
<td>240.0992</td>
<td>240.1157</td>
<td>239.9752</td>
</tr>
<tr>
<td>meanB(ADC units)</td>
<td>29.0744</td>
<td>29.4215</td>
<td>29.124</td>
<td>28.2397</td>
<td>27.7851</td>
</tr>
<tr>
<td>stdA(ADC units)</td>
<td>1.6438</td>
<td>1.6332</td>
<td>1.578</td>
<td>1.5011</td>
<td>1.4518</td>
</tr>
<tr>
<td>stdB(ADC units)</td>
<td>1.9243</td>
<td>1.9822</td>
<td>1.5087</td>
<td>1.8075</td>
<td>1.577</td>
</tr>
<tr>
<td>SNR(dB)</td>
<td>42.3084</td>
<td>42.3522</td>
<td>42.5225</td>
<td>42.9937</td>
<td>43.2964</td>
</tr>
<tr>
<td>meanA-meanB(ADC units)</td>
<td>214.4215</td>
<td>214.1157</td>
<td>210.9752</td>
<td>211.876</td>
<td>212.190</td>
</tr>
<tr>
<td>Temperature(℃)</td>
<td>6</td>
<td>2.5</td>
<td>-1</td>
<td>-3</td>
<td></td>
</tr>
<tr>
<td>meanA(ADC units)</td>
<td>239.8264</td>
<td>242.8926</td>
<td>244.405</td>
<td>242.4215</td>
<td></td>
</tr>
<tr>
<td>meanB(ADC units)</td>
<td>27.7355</td>
<td>30.1488</td>
<td>30.3058</td>
<td>28.7107</td>
<td></td>
</tr>
<tr>
<td>stdA(ADC units)</td>
<td>1.3271</td>
<td>1.2369</td>
<td>1.1873</td>
<td>1.1087</td>
<td></td>
</tr>
<tr>
<td>stdB(ADC units)</td>
<td>2.1976</td>
<td>2.0276</td>
<td>2.1635</td>
<td>1.6953</td>
<td></td>
</tr>
<tr>
<td>SNR(dB)</td>
<td>44.0721</td>
<td>44.7101</td>
<td>45.1212</td>
<td>45.7003</td>
<td></td>
</tr>
<tr>
<td>meanA-meanB(ADC units)</td>
<td>212.0909</td>
<td>212.7438</td>
<td>214.0992</td>
<td>213.7108</td>
<td></td>
</tr>
</tbody>
</table>

Table 5-1 Relation between temperature and SNR
According to Figure 5-1, the diagrams are drawn to analyze the SNR of the generated images.
From Figure 5-10, the SNR increases with the temperature decreases. In particular, when the temperature is lower than 13°C, the SNR increases more rapidly than the temperature in the range from 23°C to 17.5°C. Because of the influence of the environment temperature, which is about 23°C, the experiments are conducted in the range from 23°C to -5°C, although the datasheet provides the information for a range from -10°C to 30°C.
Temperature: 23°C

Temperature: -5°C

Figure 5-11 Histograms of region A and B

Temperature: 23°C
Temperature: -5°C

Figure 5-12 Maximum value of region A and minimum value of region B

In order to achieve a high quality evaluation, the Figure 5-11 and Figure 5-12 are posted so as to take the consideration of detector saturation which will also have an influence on the image SNR, too. The analyze will be described in the discussion part.
6 Discussion

An FPGA based real time NIR camera is developed in this thesis project. A PCB, including the considerations in relation to the logic level conversion, power source generation, analog to digital signal conversion and assembling of device, has been designed and verified successfully. VHDL implementation enables the FPGA to readout the image data from the sensor, display this on the monitor and send it to the PC. In addition, the PC software has a friendly GUI and is full of the functions required. The BMP file can be utilized in further processing.

The performance of the system has been evaluated under different temperatures. From the result, it obviously shows that the system works in a satisfactory manner. It is also the case that the SNR of images are boosted as the sensor’s temperature is decreasing. Although according to the datasheet of the NIR sensor, there is a one stage cooler available, which is able to control the sensor within the range of 30°C to -10°C, the room temperature might have an influence on that, which might be because of a too high thermal resistance in the connection of the detector metal to the cooler aluminium, which leads to the sensor temperature in the range of 23°C to -5°C during the experiments.

Then the influence of the illumination should be analyzed. The parameters drawn as shown in Figure 5-9 will assist in this analysis.

MeanA is the mean value of the region A, which is treated as the foreground and B is the background. The tendency of meanA and meanB is related to the variations of the illumination’s intensity. However, the signal=meanA−meanB still remained almost constant during the entire measurement, with only a 1.6% variation. From the tendency of stdB, it is known that the fluctuations of the background are small. However, the noise represented by stdA decreases and the signal = meanA−meanB increases as the temperature decreases. Thus the SNR boosts as in the description in the result chapter.

Figure 5-11 shows the histograms of regions A and B under the different temperatures. After zooming in on the figures, the max value and min value are the same as in Figure 5-12. Thus the max value is 246.5(3.126V), and the min value is 24.5(1.39V) in -5°C. Comparing these
with the values at 23°C, it is thus known that the detector is saturated at -5°C. According to the Formula-1, meanA will abate leading to a reduction of the SNR.

Additionally, based on the limited conditions, the investigation was conducted without measuring the temperature of the sensor. The resistance of thermal resistor was measured in order to obtain the chip temperature and then the results were recorded. In addition, the experiments for the SNR investigation should avoid solar light. However, the summer night is short while the experiments took a long time and thus the evaluation of the SNR images under the variation of temperature proved not to be as successful as was hoped.

In relation to the aim of detecting the ice or water covering on the road surface, the experiments should be conducted in the future to attempt to detect that by analyzing the images received. After verification, the method will be integrated into the FPGA platform.
7 Conclusions

With regards to the aim of exploiting a system for monitoring the ice/water on road surface, the thesis has drawn an approach to develop a hardware device based on NIR technology.

The NIR image sensor requires high speed processing which is able to be managed by FPGA. The whole system contains three parts, including the interface PCB, FPGA processing and host PC software. All the implementations are described in the paper. The parts are accomplished separated, and then the combination is performed successfully.

From the experiments, in general, the system does achieve the purpose in relation to the building of the hardware structure. From the result, the objects exist in the bmp image in accordance with the expectation. The evaluation experiments were performed by utilizing a one stage cooler, which was integrated into the NIR sensor. How the cooler affects on the SNR images can also be studied. A metal base, will have an influence on the system temperature uniformity, based on its thermal conductivity, which was used to fix the system. However, it will enhance the system performance.

A future continuance of this work should be to place the system into a practical situation in which more disturbance factors exit. In addition, the images stored in the PC should be analyzed by some method in order to have knowledge as to that whether the ice/water is able to be classified. Finally, the method may be applied into the FPGA platform to make the system achieve the final goal.
References

[1] Swedish Road Administration, “Road weather information system”


[14] “InGaAs area image sensor”, Hamamatsu, Sep, 2011


http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,836&Prod=ATLYS December 19, 2011
Appendix A: Documentation of own developed program code

VHDL code for NIR sensor reading (NIRReadout)

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
-- use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity NIRReadout is
  Port ( ADCLK : in  STD_LOGIC;
         MSP  : in   STD_LOGIC;
         ADTrigger : in  STD_LOGIC;
         RowStart  : out STD_LOGIC;
         ADData : in  STD_LOGIC_VECTOR (11 downto 0);
         PData : out  STD_LOGIC_VECTOR (11 downto 0));
end NIRReadout;

architecture Behavioral of NIRReadout is

begin

readout: process( ADCLK)

  variable RowCount : integer := 0;
  variable ColCount : integer := 0;
  variable ReadCount : integer := 0;  ---- For delay of AD conversion
  variable PixelCount : integer := 0;
  variable StartCount : STD_LOGIC := '0';
  variable agoFlag : STD_LOGIC := '0';


variable ADtmp : STD_LOGIC_VECTOR (11 downto 0) :=
(others=>'0');

begin

if(ADCLK'event and ADCLK = '0') then
    if (MSP = '0') then    ---- Reset signals and variables
        RowCount := 0;
        ColCount := 0;
        agoFlag := '1';
        StartCount := '0';
        ReadCount := 0;
    end if;

    if (ADTrigger = '1') then  ---- Detecting falling edge
        agoFlag := '1';
    elsif(ADTrigger = '0') then
        if(agoFlag = '1') then
            agoFlag := '0';
            StartCount := '1';
            ReadCount := 0;
        end if;
    end if;
end if;

if StartCount = '1' then
    if(ReadCount <= 100) then  -- Avoid ReadCount overflow
        ReadCount := ReadCount + 1;
    end if;
    if ReadCount = 7 then      ----7 is wait cycles for AD conversion
        StartCount := '0';
        ADtmp := ADDATA;
    end if;
ColCount := ColCount + 1;
if(ColCount = 1) then
    RowCount := RowCount + 1;
    if RowCount>= 2 then
        RowStart <= '1';
    end if;
elsif(ColCount = 64) then  ----- ColCount := 0;
RowStart <= '0';
end if;

end if;
end if;

PData <= ADtmp;
end if;
end process;

end Behavioral;

Pixels of NIR image generation (videoGen.vhd)

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity NIRReadout is
    Port ( ADCLK : in  STD_LOGIC;
            MSP : in   STD_LOGIC;
            ADTrigger : in  STD_LOGIC;
            RowStart  : out STD_LOGIC;
            AData : in  STD_LOGIC_VECTOR (11 downto 0);
            PData : out  STD_LOGIC_VECTOR (11 downto 0));
end NIRReadout;

architecture Behavioral of NIRReadout is

begin

readout: process( ADCLK)
variableRowCount : integer := 0;
variableColCount : integer := 0;
variableReadcount : integer := 0; ---- For delay of AD conversion
variablePixelCount : integer := 0;
variableStartCount : std_logic := '0';
variableAgoFlag : std_logic := '0';
variableADtmp : std_logic_vector (11 downto 0) :=
(others=>'0');

begin

if(ADCLK'event and ADCLK = '0') then
    if (MSP = '0') then ---- Reset signals and variables
        RowCount := 0;
        ColCount := 0;
        agoFlag := '1';
        startCount := '0';
        ReadCount := 0;
    end if;

    if (ADTrigger = '1') then ---- Detecting falling edge
        agoFlag := '1';
    elsif(ADTrigger = '0') then
        if(agoFlag = '1') then
            agoFlag := '0';
            StartCount := '1';
            ReadCount := 0;
        end if;
    end if;
end if;

if StartCount = '1' then
    if(ReadCount <= 100) then -- Avoid ReadCount overflow
        ReadCount := Readcount + 1;
    end if;
    if ReadCount = 7 then -----7 is wait cycles for AD
        startCount := '0';
        ADtmp := ADDATA;
    end if;
end if;
if(ColCount = 1) then
    RowCount := RowCount + 1;
    if RowCount>= 2 then
        RowStart <= '1';
    end if;
elsif(ColCount = 64) then
    ColCount := 0;
    RowStart <= '0';
end if;
end if;

PData <= ADtmp;
end if;
end process;

end Behavioral;

**VB software code**

'Author: Haoming Zeng

'Create Date: 2012-07-01

'Description: 1. The software is able to receive data via UART.
    2. plot the image in the form
    3. save the image as BMP file.

'Additional Comments: For more information, please check specification

Dim Hstrbuffer As String
Dim strData As String
Dim strlen As Integer
Dim ReceiveCount As Integer
Dim ReceiveCountH As Integer

Dim dRow, dCol As Integer

Dim Index As Integer

Dim imgWidth As Integer    ' the width of image
Dim imgHeight As Integer   ' the height of image

Private Sub Command1_Click()    ' Start command
  Dim a As Integer

  dRow = 0
  dCol = 0

  imgWidth = CInt(Text1.Text)
  imgHeight = CInt(Text2.Text)

  Picture1.Width = imgWidth + 4    ' 4 is for boundry
  Picture1.Height = imgHeight + 4
  Picture1.ScaleMode = 3
  Picture1.AutoRedraw = True

  If (Combo1.ListIndex > -1) Then
FPAG based smart NIR camera

Haoming Zeng

Appendix A: Documentation of own developed program code

2012-11-29

MSComm1.CommPort = Combo1.ListIndex + 1 '...Set port according to the choise

MSComm1.Settings = Combo3.Text & ",n,8,1" '...Communication parameters

MSComm1.InputMode = comInputModeBinary 'Binary mode for receive buffer

'MSComm1.InputLen = 0

MSComm1.InBufferSize = 20000 ' Set InputBuffer size to 30000 bytes
MSComm1.OutBufferSize = 2 ' Set InputBuffer size to 2 bytes
MSComm1.InBufferCount = 0 ' Empty inputbuffer
MSComm1.OutBufferCount = 0 ' Empty outputbuffer
MSComm1.SThreshold = 0 'Close empty buffer trigger the uart interrupt sevice
MSComm1.RThreshold = 0 ' Close Every X bytes trigger the uart interrupt sevice

MSComm1.PortOpen = True '..Open port

Command1.Visible = False

Combo1.Enabled = False

Combo3.Enabled = False


TmrComm.Enabled = True ' Start timer

dRow = 0
dCol = 0

Command4.Visible = True  'Set reset button visible

Else

    a = MsgBox("Please choose a com port!", 1, "OK")

End If

End Sub

Private Sub hexReceive()

Dim ReceiveArr() As Byte  'Receive array
Dim receiveData As String  'Temp variable for receive data
Dim Counter As Integer  'Count the numbers of data received
Dim i As Integer       'For Loop index

If (MSComm1.InBufferCount > 0) Then
    Counter = MSComm1.InBufferCount  'How many datas totally
    receiveData = ""               'Clear temp
    ReceiveArr = MSComm1.Input  'Put data from buffer to array
    For i = 0 To (Counter - 1) Step 1
        If (ReceiveArr(i) < 16) Then
            receiveData = receiveData & "0" + Hex(ReceiveArr(i)) & Space(1)  'If the data smaller than 16, then add a '0' (for HEX display)
        Else
            receiveData = receiveData & Hex(ReceiveArr(i)) & Space(1)  'Add a space for display
        End If

        'If (ReceiveArr(i) <> 128) Then
        '    TxtReceive.Text = TxtReceive.Text + receiveData  'Display in text box
        '    TxtReceive.SelStart = Len(TxtReceive.Text)  'Show the cursor's place
        'End If

    Next i
End If
Picture1.PSet (dCol, dRow), RGB(CInt(ReceiveArr(i)), CInt(ReceiveArr(i)), CInt(ReceiveArr(i))) 'Draw pixel

'Picture1.PSet (dRow, dCol), CInt(ReceiveArr(i))         'Draw pixel

dCol = dCol + 1

If dCol = imgWidth Then

dCol = 0

dRow = dRow + 1

If dRow = imgHeight Then

    dRow = 0
    SavePicture Picture1.Image, "c:\NIR" & CStr(Index) & ".bmp"
'Save into bmp file
    Index = Index + 1

End If
End If

Next i
TxtReceive.Text = TxtReceive.Text + receiveData ' Display in text box
TxtReceive.SelStart = Len(TxtReceive.Text) ' Show the cursor's place
End If

'---------------------------------------------------------------------
'This counter will lead to software crash
'if the PC in bad condition (such as too much software running at the same time)
'---------------------------------------------------------------------

ReceiveCount = ReceiveCount + Counter ' Count how many datas received in total

If ReceiveCount > 10000 Then 'Due to one integer can not display a value which out of range
ReceiveCount = ReceiveCount - 10000
ReceiveCountH = ReceiveCountH + 1

If ReceiveCount > 10000 Then
    ReceiveCount = ReceiveCount - 10000
    ReceiveCountH = ReceiveCountH + 1
End If

If ReceiveCountH > 30000 Then
    ReceiveCountH = 0
End If
End If

txtRXcount.Text = "RX:" & ReceiveCountH & "x10000+" & ReceiveCount
' Display RX in the format of num*1000 plus num

End Sub

Private Sub Command3_Click()

SavePicture Picture1.Image, "c:\NIR" & CStr(Index) & ".bmp"
Index = Index + 1

    dRow = 0
dCol = 0

    Picture1.Picture = LoadPicture()

End Sub

Private Sub Command4_Click() 'Reset command

MSComm1.PortOpen = False
Command1.Visible = True

ReceiveCount = 0
ReceiveCountH = 0

Combo1.Enabled = True
Combo3.Enabled = True

Label4.Caption = "Now you can reconfigure the parameters"    ' Show the current state

Command4.Visible = False

TmrComm.Enabled = True
' Start timer

End Sub

Private Sub Send_Click()

TmrComm.Enabled = False

ReceiveCount = 0
ReceiveCountH = 0

Picture1.Picture = LoadPicture()

If MSComm1.PortOpen = True Then ' If uart port open

    MSComm1.InputMode = comInputModeText ' Set the send out mode to text
    MSComm1.Output = Trim("w")          ' send out 'w'

    DoEvents
    Loop Until MSComm1.OutBufferCount = 0    'wait

    MSComm1.Output = ""
    ModeSend = False
    MSComm1.InBufferCount = 0
    MSComm1.InputMode = comInputModeBinary

Else
MsgBox "Port is closed, please open it", 48, "NIR Pro" ' Warning for Port not open
End If

TmrComm.Enabled = True

End Sub

Private Sub TmrComm_Timer() ' Every preset time arriving (Set the interval parameter of Timer)

Dim Rx_buff() As Byte
Dim okstring As String
Dim ReceivedLen As Integer

TmrComm.Enabled = False ' Close timer

If MSComm1.InBufferCount > 0 Then ' Check receive buffer
    Call hexReceive
End If
TmrComm.Enabled = True ' Open timer
End Sub

Private Sub Command2_Click() ' For QUIT

'...Quit

Unload Me

End Sub

Private Sub Form_Load() ' When the form is loaded

Combo1.AddItem "COM1"
Combo1.AddItem "COM2"
Combo1.AddItem "COM3"
Combo1.AddItem "COM4"
Combo1.AddItem "COM5"

Combo1.AddItem "COM6"
Combo1.AddItem "COM7"
Combo1.AddItem "COM8"
Combo1.AddItem "COM9"
Combo1.AddItem "COM10"
Combo1.AddItem "COM11"
Combo1.AddItem "COM12"
Combo1.AddItem "COM13"
Combo1.AddItem "COM14"
Combo1.AddItem "COM15"
Combo1.AddItem "COM16"

Combo3.AddItem "9600"
Combo3.AddItem "38400"
Combo3.AddItem "115200"
Combo3.AddItem "256000"

Command4.Visible = False

Index = 0

dRow = 0
dCol = 0

End Sub