Performance of CMOS and Floating-Gate Full-Adders Circuits at Subthreshold Power Supply

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Abstract. To reduce power consumption in electronic designs, new techniques for circuit design must always be considered. Floating-gate MOS (FGMOS) is one of those techniques and has previously shown potentially better performance than standard static CMOS circuits for ultra-low power designs. One reason for this is because FGMOS only requires a few transistors per gate and still retain a large fan-in. Another reason is that CMOS circuits becomes very slow in subthreshold region and are not suitable in many applications while FGMOS can have a shift in threshold voltage to increase speed performance. This paper investigates how the performance of an FGMOS full-adder circuit will compare with two common CMOS full-adder designs. Simulations in a 120 nm process shows that FGMOS can have up to 9 times better EDP performance at 250 mV. The simulations also show that the FGMOS full-adder is 32 times faster and have two orders of magnitude higher power consumption than that for CMOS.

1. Introduction

It has become more and more important to reduce the power consumption in circuits while still trying to achieve as high switching speed as possible. The increasing demands for longer lasting lifetimes in portable and battery driven applications are some of the strongest driving forces to push the limits in terms of ultra-low power consumption. According to the ITRS Roadmap for Semiconductors [18], the two most important of the five “grand challenges” for future nanoscale CMOS are to reduce power consumption and design for manufacturability. In this work we have chosen to focus on reducing power consumption. The challenge to design for manufacturability is desirable for future work within this topic.

One of the ways to reduce power is to explore new types of circuits in order to find better circuit techniques for energy savings. Floating-gate MOS (FGMOS) is a circuit technique that has been proposed in several previous works as a potentially good technique to reduce power consumption and still maintain a relatively high speed [1],[2],[3]. FGMOS is normally fabricated using a standard CMOS process where an extra floating-gate capacitance is connected to the transistor’s gate node. This capaci-

tance, called floating-gate capacitance, will make it possible to shift the threshold voltage level of the MOS-transistors. The required effective threshold voltage for the gate will thereby change and the shift is controlled by the floating-gate's node charge voltage [1],[3]. A shift in threshold voltage will also change the static current (and power consumption), normally to a higher value, at the same time as the propagation delay of the circuit will be different (normally smaller).
Maximum propagation delay, t_p, and power consumption of a circuit, P, are two figures of merits that are important in FGMOS designs. These figures must be considered while simulating with different fan-ins. In our simulations we have been using power consumption (P), power-delay product (PDP) and energy-delay product (EDP) as figure of merits to determine differences in performance [4].
The approach to reduce power consumption and increase performance in this work is to lower the circuits power supply voltage into subthreshold region.
Previous works in this area have shown that FGMOS circuits working in subthreshold should not have a fan-in higher than 3 in order to be able to have advantages compared to CMOS [14]. This advice has been taken into account in this work where we use an FGMOS full-adder with a maximum fan-in of 3 and compare it to two common basic CMOS full-adders with respect to power and speed performances.
The aim of this work has been to determine if the FGMOS full-adder will show better performance than normal CMOS full-adders when power supply is reduced below subthreshold voltage. This is important knowledge since subthreshold designs have been frequently proposed to be good for ultra-low power consumption [19].
In this article we show that when the power supply is reduced into subthreshold region (250 mV), the FGMOS circuits will have up to 9 times better EDP and 32 times higher speed than the CMOS circuits. However, FGMOS will also have penalty with over two orders of magnitude higher power consumption and also worse PDP.

2. FGMOS Basics

The FGMOS technique is based on normal MOSFET transistors and CMOS process technology. They are manufactured with an extra gate capacitance in series with the transistor's gate. Because of that, FGMOS can shift the effective threshold potential required by the transistor. The shifts in the threshold are made by charging the node between the extra gate capacitance and the normal transistor gate. If there is no charge leakage, the node is said to be floating and it is called a true floating-gate circuit. The added extra capacitance is called a floating-gate capacitance (C_{FG}). Figure 1 shows a floating-gate transistor and a majority gate with fan-in 3 designed in FGMOS.
Depending on the size of the floating-gate charge voltage (V_{FG}), the effective threshold voltage will vary. V_{FG} is determined during the design process and the floating-gate circuits are subsequently programmed with the selected V_{FG} once and then they are fixed during operation [6].
Implementation of the floating-gate potential, V_{FG}, can be made via a variety of different methods. For true floating-gates, hot-electron injection, electron tunnelling or UV-exposure is normally used [3],[10],[11]. If the CMOS process also has a gate-

oxide thickness of 70Å or less [7], some kind of refresh or auto-biasing technique is also required as gate charge leakage will be significant [8].

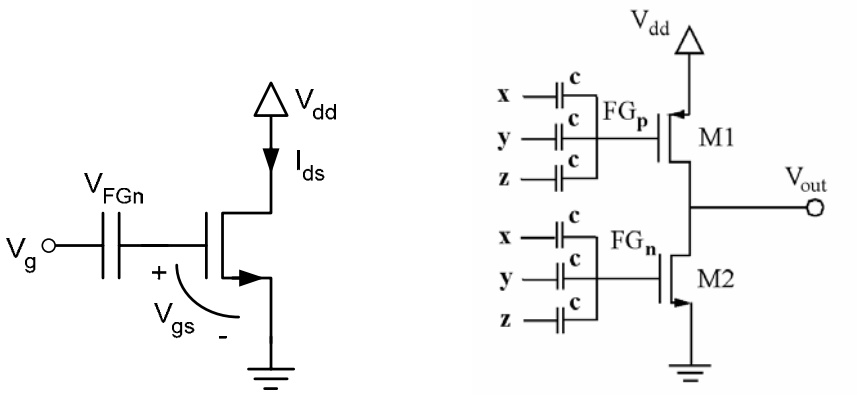

Figure 1. FGMOS transistor (left) and FGMOS Majority-3 gate with fan-in 3 (right).

3. Full-Adder Designs

The Full-adder is one of the most used basic circuits since addition of binary numbers are one of the most used operations in digital electronics. Full-adders exist everywhere in electronic systems and a large amount of research has been done in this area in order to achieve best possible performance [12], [13], [15].
There exist many different solutions for full-adder designs, this work have focused on two the most commonly used basic CMOS full-adders. A standard static CMOS full-adder design (Figure 4) and a mirrored–gate based full-adder (Figure 3) have been used in our simulations to determine speed and power performance compared to a floating-gate full-adder. The floating-gate full-adder is represented by a recently improved adder structure with a maximum fan-in of 3 [14]. This full-adder is shown in Figure 2 and have shown potential to be better than CMOS at subthreshold.

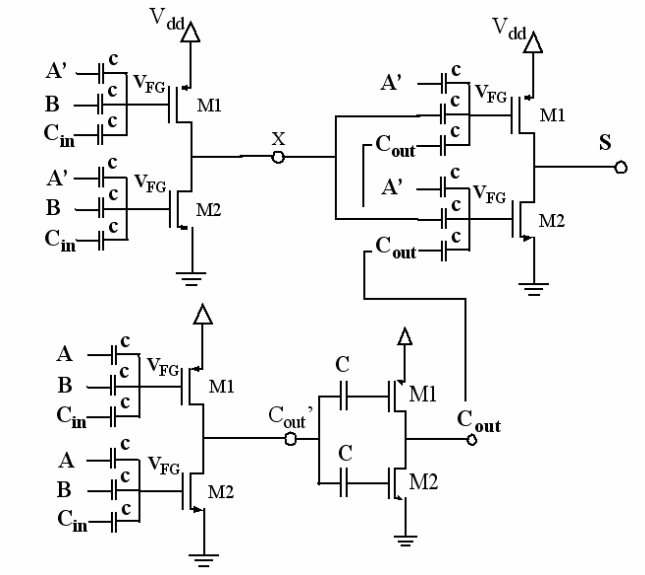

Figure 2. FGMOS full-adder with fan-in 3

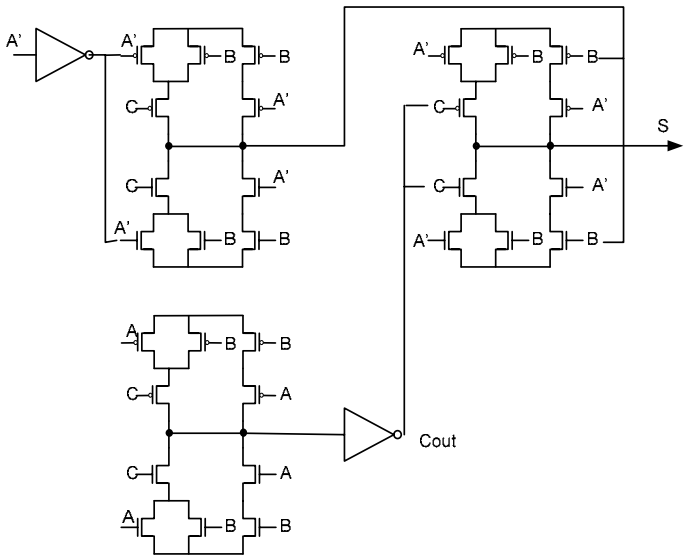

Figure 3. Mirrored CMOS full-adder.

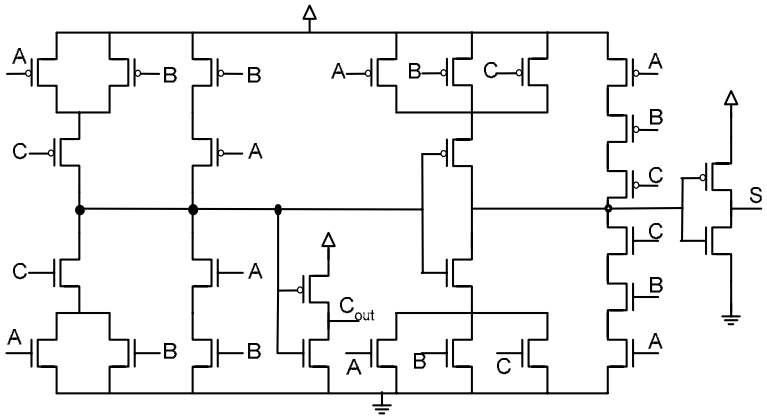

Figure 4 . Standard static CMOS full-adder.

4. Full-Adder Simulations

The simulations have been performed in Cadence with the Spectre simulator in a 120 nm CMOS process technology and the used transistors are of low-leakage type. The transistors using minimum gate lengths, 120 nm (effective), and a width of 150 nm for NMOS and a width of 380 nm for the PMOS. The threshold voltage, V_{th}, for these low-leakage transistors are 383 mV for NMOS and -368 mV for PMOS according to the simulations.

Previous research with full-adders at subthreshold power supply, suggests that the EDP performance for FGMOS can be better than EDP for CMOS if the fan-in of the floating-gate circuit is below four [14]. For this reason, a floating-gate full-adder structure with a fan-in of three has been used.

In this work the simulations have been performed for three types of full-adders, one FGMOS and two CMOS. The power supply for the simulations are chosen between 150 mV - 250 mV since previous simulations have shown that this is the range in subthreshold with best performance. The propagation delay, t_p, for a full-adder varies with every different state change on the input and because of that, the results from our simulations are based on the slowest input to output change [15].

EDP is calculated from the average power consumption (P) and the minimum signal propagation delay, t_p, according to Eq. 1. It is the consumed power required to drive the output to 90% of its final value multiplied by the propagation delay squared.

Eq. 1 $$EDP = PDP \cdot t_p = I_{avg} \cdot V_{dd} \cdot t_p \cdot t_p = P \cdot t_p^2$$

I_{avg} is the average switching current and t_p is the inverter's minimum propagation delay [4].

5. Results

The simulation results from this work should determine if FGMOS can be used to design better full-adder circuits than static and mirrored CMOS. Figure 5 and Figure 6 show plots of EDP for the circuits at 150 mV and 250 mV power supply. As seen, the EDP can be up to 9 times better for FGMOS at 250 mV depending on how you chose the floating-gate voltage V_{GFp}. In all the figures we have plotted CMOS' EDP as straight horizontal lines to be easily comparable with FGMOS.

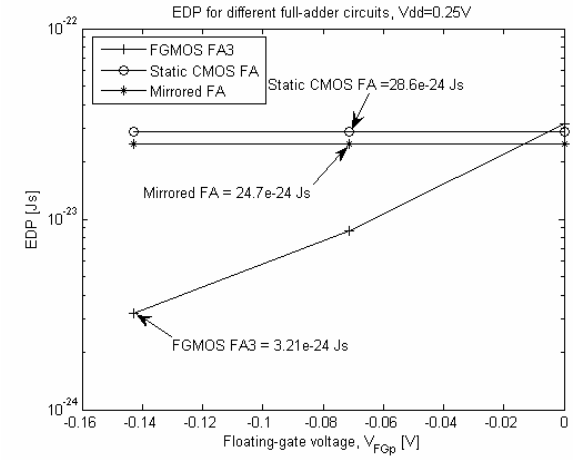

Figure 5. EDP for Floating-gate and CMOS full-adders at 250 mV

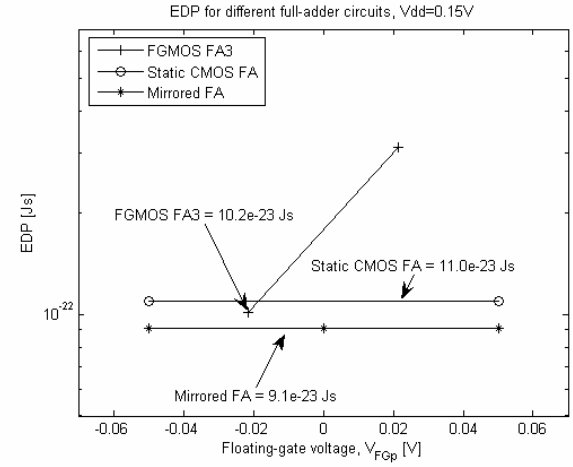

Figure 6. EDP for Floating-gate and CMOS full-adders at 150 mV.

The plots show the limit of how large the floating-gate voltage can be while the circuit's gain is higher than one. If the floating-gate voltage, V_{FGp}, is set more negative than in these plots, there will be an attenuation of the signal for each gate.

Figure 7 shows the PDP (at 250 mV) which is almost constant for all applied different floating-gate voltages and is approximately 4 times worse than PDP for each of the CMOS full-adders. Similar results can be obtained from simulations at 150 mV.

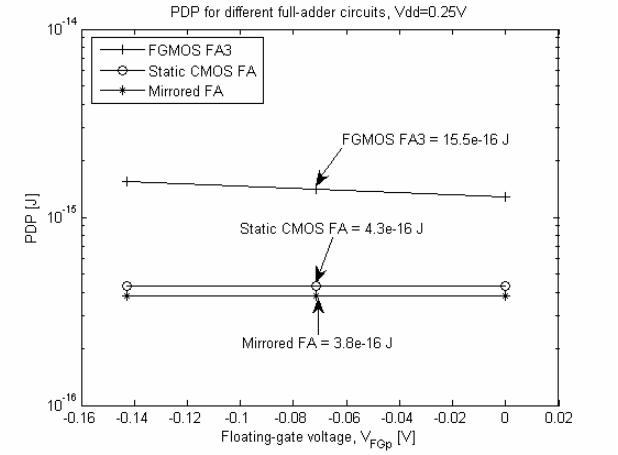

Figure 7. PDP for different full-adders at 250 mV power supply.

Plots from the simulations of propagation delay can be seen in Figure 8 and Figure 9 and the FGMOS full-adder has up to 33 times shorter delay compared to the CMOS versions at 250 mV.

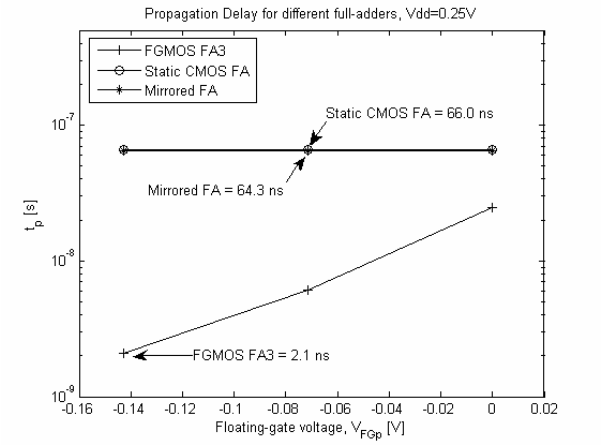

Figure 8. Propagation delay for the different full-adders at 250 mV. The horizontal lines are for the CMOS circuits.

Figure 10 shows the power consumption at 250 mV and it is more than two orders of magnitude higher for FGMOS (114 times).

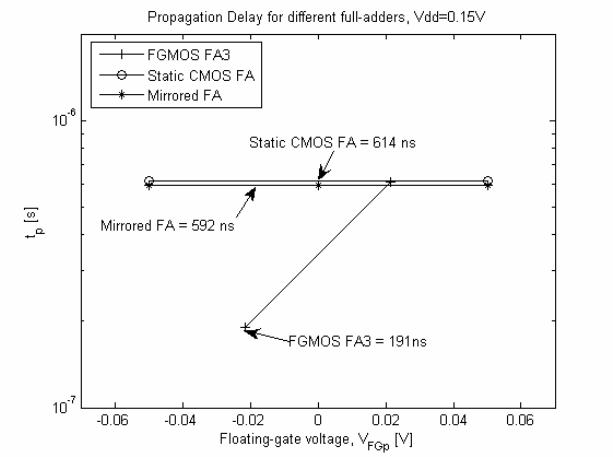

Figure 9. Propagation delay for the different full-adders at 150 mV. The horizontal lines are for the CMOS circuits.

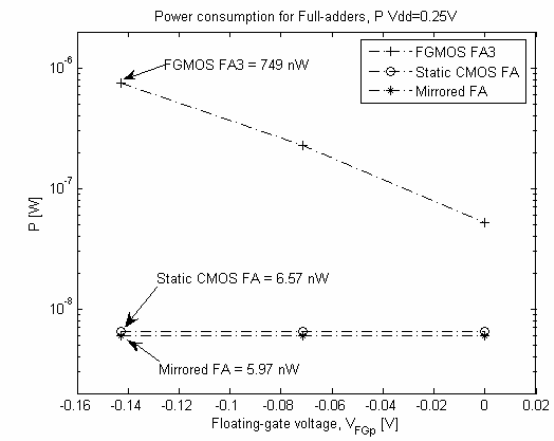

Figure 10. Power consumption for the three types of full-adders.

6. Discussion

FGMOS circuits have in previous studies shown that it can achieve better EDP performance in subthreshold region than normal static CMOS and the fan-in should not be more than three [2],[14]. While there is an advantage in EDP performance for FGMOS in subthreshold, there is also a penalty with a worse PDP and power consumption that needs to be taken into account.

The simulation results in this work shows that the EDP can be up to 9 times better for FGMOS full-adder compared to the static CMOS design. It also shows an advantage

in switching speed that is 33 times higher for FGMOS than for CMOS full-adders at 250 mV. Even at 150 mV, the switching speed will be more than 3 times better for FGMOS.
The mirrored CMOS and static CMOS full-adder circuits in this work have been chosen to be compared with FGMOS since they have shown to have some of the best results of commonly used full-adders in terms of P, PDP and EDP[12],[13]. To notice is also that the mirrored gate full-adder has better performance than the static CMOS full-adder in all the three figures of merits.
Even though the results from simulations performed in this work shows a clear advantage for FGMOS when certain design constraints are fulfilled, it must be taken into account that it might not be possible to design the FGMOS with a true floating-gate. It could be required to use some kind of refresh circuit, either as a large resistance or switch that retain or recharge the voltage on the floating-gate node [16],[17]. This will of course have an impact on performance. Especially for state-of-the-art and future process technologies where the gate-oxide thickness decreases for every generation this will be an issue to carefully look into during the design process.
There is still a lot of research to be done within the field of subthreshold FGMOS to find out more advantages or limitations. Some work close related to the topic of this article could be to do a more detailed analysis of netlists from layout perform real measurements. It would also be interesting to find out how statistical process variations and mismatches between components will affect the performance.

7. Conclusions

Using FGMOS circuits in subthreshold power supply can give several times improvement in terms of EDP and over one order of magnitude better gate propagation delay than comparable CMOS circuits.
These advantages in performance will hopefully lead to more ultra-low power circuits with higher requirements on switching frequency.
While the FGMOS circuits can be much faster and have better EDP than CMOS, they will also have significantly higher power consumption than and that will on the other hand decrease the number of possible applications for FGMOS. The performance constraints for FGMOS designs in subthreshold, especially the power consumption, will be one of the major limiting factors that decide if floating-gate circuits can be used in a specific design.

8. References

[1] T. Shibata and T. Ohmni, “A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations,” *IEEE Transactions on Electron Devices 39,* 1992.

[2] J. Alfredsson, S. Aunet and B. Oelmann, “Basic speed and power properties of digital floating-gate circuits operating in subthreshold,” *IFIP VLSI-SOC 2005, Proc. of IFIP International Conference on Very Large Scale Integration,* Australia, Oct 2005.

[3] P. Hasler, T. S. Lande, "Overview of floating-gate devices, circuits and systems," *IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol.48, No.1, January 2001.

[4] M. R. Stan, "Low-power CMOS with subvolt supply voltages," *IEEE Transactions on VLSI Systems*, Vol.9, No.2, April 2001.

[5] E. Rodríguez-Villegas, G. Huertas, M. J. Avedillo, J. M. Quintana and A. Rueda, "A Practical Floating-Gate Muller-C Element Using vMOS Thershold Gates," *IEEE Transactions on Cirucits and Systems-II: Analog and Digital Signal Processing*, Vol. 48, No.1, January 2001.

[6] S.Aunet, Y. Berg, T. Ytterdal, Ø. Næss, T. Sæther, "A method for simulation of floating-gate UV-programmable circuits with application to three new 2-MOSFET digital circuits," *The 8th IEEE International conference on Electronics, Circuits and Systems*, Vol.2, pp. 1035-1038, 2001.

[7] K. Rahimi, C. Diorio, C. Hernandez and M.D. Brockhausen, "A simulation model for floating-gate MOS synapse transistors," ISCAS2002, *Proc. of the 2002 IEEE International Sympposium on Circuits and Systems*, Vol.2, pp. 532-535, May 2002.

[8] J. Ramírez-Angulo, A.J. López-Martín, R. González Carvajal and F. Muñoz Chavero, "Very low-voltage analog signal processiing based on quasi-floating gate transistors," *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 3, pp. 434-442, March 2004.

[9] G. Schrom and S. Selberherr, "Ultra-Low-Power CMOS Technologies," Invited paper, *Proc. of International Semiconductor Conference*, Vol. 1, pp. 237-246,1996.

[10] S. Aunet, "Real-time reconfigurable devices implemented in UV-light programmable floating-gate CMOS," Ph.D. Dissertation 2002:52, Norwegian University of Science and Technology, Trondheim, Norway, 2002.

[11] J. M. Rabaey, "Digital Integrated Cirucuits - A design perspective", ISBN 0-13-120764-4, pp. 188-193, Second edition, Prentice Hall, 2003.

[12] M. Alioto and G. Palumbo, "Impact of Supply Voltage Variations on Full Adder Delay: Analysis and Comparison," *IEEE Transactions on very large scale integration (VLSI) systems*, Vol.14, No.12, December 2006.

[13] K. Granhaug and S. Aunet, "Six Subthreshold Full Adder Cells characterized in 90 nm CMOS technology," *Design and Diagnostics of Electronic Circuits and Systems*, pp.25-30, IEEE, April 2006.

[14] J. Alfredsson, S. Aunet and B. Oelmann, "Small Fan-in Floating-gate Circuits with Application to an Improved Adder Structure," *Proc. of 20th international Conference on VLSI design*, Bangalore, India, January 2007.

[15] A. M. Shams and M. A. Bayoumi, "A Framework for Fair Performance Evaluation of 1-bit Full Adder Cells," *42nd Midwest Symposium on Circuits and Systems*, Vol.1 pp.6-9, August 1999.

[16] I. Seo and R. M. Fox, "Comparison of Quasi-/Pseudo-Floating Gate Techniques" *Proceedings of the International Symposium on Circuits and Systems, ISCAS 2004*, Vol. 1, pp.365-368, May 2004.

[17] J. Alfredsson and B. Oelmann, "Influence of Refresh Circuits Connected to Low Power Digital Quasi-Floating gate Designs," P*roceedings of the 13th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2006*, Nice, France, December 2006.

[18] International Technology Roadmap for Semiconductors, Webpage documents http://public.itrs.net

[19] T. S. Lande, D. T. Wisland, T. Sæther and Y. Berg, "Flogic – Floating Gate Logic for Low-Power Operation", Proceedings of International Conferens on Electronics Circuits and Systems, ICECS'96, vol.2, pp.1041-1044, April 1996.