D-latch for Subthreshold Floating-Gate Circuits Exploiting Threshold Elements

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Abstract - When power supply for circuits is reduced the performance will also drop accordingly and to keep up the performance while lowering power supply is an important issue. Floating-gate circuits (FGMOS) have previously been simulated with low power supply and basic digital gates and circuits have already been designed and studied to determine speed and power performance. In this paper we try to expand the circuit library for subthreshold power supply FGMOS circuits by including a floating-gate memory element in terms of a D-latch. Our simulations at 250 mV power supply of a FGMOS D-latch are compared with other D-latches based on static CMOS and mirrored gate elements. The simulations we have performed shows that static CMOS has an advantage in performance of several orders of magnitude in terms of power consumption, while PDP and EDP performance are also better than for FGMOS. When it comes to speed performance, we show that the FGMOS D-latch can be up to 18 times faster than CMOS at the expense of up to three orders of magnitude higher power consumption.

I. INTRODUCTION

Reducing the power and still maintain performance of the circuit is important in many electronic designs. With the all time increasing demand for portable, battery driven applications that consumes low power, the market needs to explore new types of circuits in order to find better techniques to use for high performance low-power applications.

Floating-gate MOS (FGMOS) is a technique that when power supply is decreased to reduce power consumption and still maintain a relatively high speed. The reduction in power is achieved when the circuits power supply voltage is reduced [1],[2]. FGMOS is a technique that has an advantage that it can work at a higher speed and have better EDP than CMOS for basic digital circuits with subthreshold power supply [2].

FGMOS circuits also have an advantage in that they can be fabricated using a standard CMOS process where an extra floating-gate capacitance is connected to the transistor's gate node. This capacitance, called floating-gate capacitance, C_{FG}, will make it possible to shift the threshold voltage level of the MOS-transistors by deposit a charge on the FG-node and thereby achieve better performance [1],[3]. Figure 1a shows a floating-gate transistor with the floating-gate capacitance.

The aim of this work has been to find out subthreshold performance of a D-latch designed in FGMOS and compare it to similar designs in static CMOS. With a D-latch in the FGMOS catalogue of circuits working in subthreshold we will be able to design finite state machines in addition to combinatorial logics and systems that we have been able to design with our previously characterized building blocks.

II. FGMOS CIRCUITS

Floating-Gate circuits have been used almost since the introductions of the MOSFET transistors but it is in the past 15 years it have had a more widely spread area of Applications [1],[3],[5]. Since the MOSFET has its gate isolated from the channel, researchers discovered that this could be used to make the transistors functional in a wider range of different supply voltages by using floating-gate technique (FGMOS) to change the effective threshold voltages. FGMOS are manufactured as ordinary CMOS-transistors with an extra gate capacitance in series with the normal transistor gate to create a floating-gate node isolated from its surroundings. Charging this node will introduce a static shift to the applied signals which will affect the conductivity of the transistors. This is especially important when the transistor is in subthreshold mode and have very low conductivity.

FGMOS-transistors can be fabricated in a normal CMOS process which is also of great importance to ensure high production capacity at as low cost as possible. The floating-gate techniques are then able to change performance of the circuits significantly.

Depending on how high the floating-gate voltage (V_{FG}) are, the effective threshold voltage for the circuit will be adjusted accordingly. One of the easiest ways to determine proper V_{FG}s for a specific circuit is to do simulations with a previous designed balancing scheme [4]. The circuit will be in balance when V_{FG} have been chosen so that an input signal of Vdd/2 gives an output signal of Vdd/2. When V_{FG} has been selected, it will normally be fixed for the circuit during

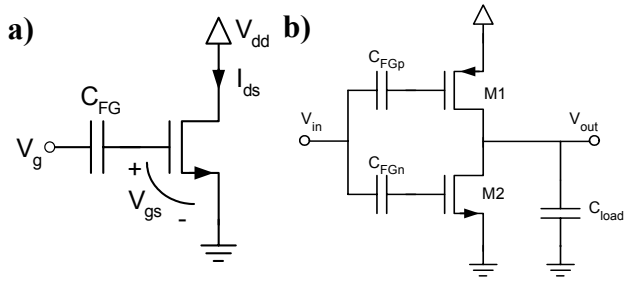

Fig. 1 a) Floating-gate nMOS transistor.
b) Ideal FGMOS inverter.

its operational lifetime [4]. Programming of the V_{FG} can be made via a variety of different methods. The most common are hot-electron injection, Fowler-Nordheim electron tunnelling and UV-exposure [1]. Figure 1b shows an ideal FGMOS-inverter.

FGMOS circuits that have no charge leakage are normally called true Floating-Gate circuits. In reality, every FG circuit will have a little leakage even if it is very small and floating-gate circuits have traditionally been manufactured for long-term storage of information since the floating-gate charges are intended to be retained permanently or until reprogramming.

For future process technologies where the transistor-gate thickness will bethinner, for example when it comes to CMOS processes with gate-oxide thickness of 70Å or less [5], some kind of refresh or auto-biasing technique has to be used as the gate leakage will have a significant influence on performance [6]. Discovery of new isolating materials may also play an important role in reducing gate-leakage currents in the future.

III. D-LATCH IN FGMOS

Floating-gate circuits have the advantage compared to other digital design techniques that all basic digital gates can be designed with only 2 transistors each and a number of floating-gate capacitances that are representing the fan-in [9]. We have previously published research in this area [2][10] where we suggests that the best subthreshold FGMOS performance compared to CMOS can be achieved at 250 mV with a maximum fan-in of 3. In order to get comparable results for the D-latches described in this work we have therefore been choosing the power supply and fan-in according to those previous results.

The topology for the D-latch used in this work is based on a previously used topology with fan-in 5 [9],[7] that has been redesigned. The new design is based on a 3-input FGMOS threshold elements and which can be configured to all basic types of digital gates [8]. The new design should give improved noise margin and the possibility for the circuit to work at lower power supply than the previous version.

The basic building block in the FGMOS design is the Majority-3 gate that can be seen in Fig. 2a. and based on that

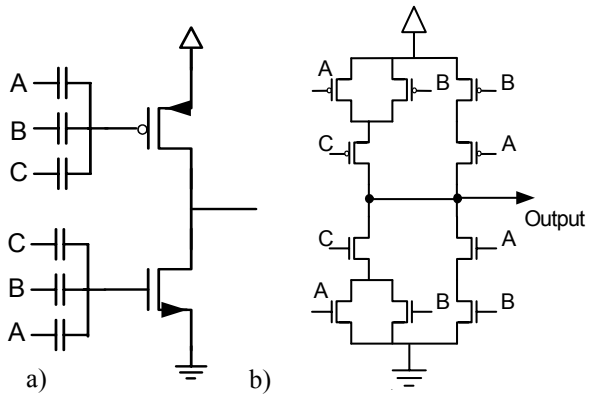

Fig. 2a)Floating-gate Majority-3 gate
b)Mirrored Gate element with fan-in 3.

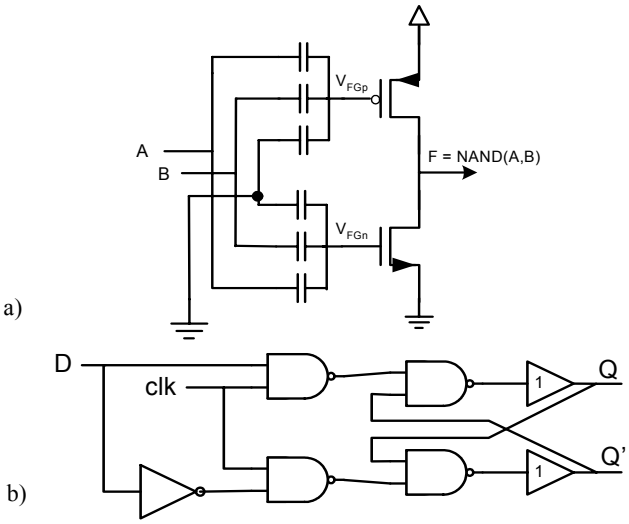

Fig. 3.a) 2-input NAND gate created in FGMOS
b.) D-Latch topology for FGMOS implementation.
1 inverter, 4 NAND-gates and 2 buffers

it is possible to design different types of digital gates [8]. For example, a 2-input NAND gate can be created by grounding one of the inputs, see Fig. 3a.

The basic building blocks for the D-latch we use in our simulations are NAND-gates, digital inverters and buffers and in order to get an overview on how good the FGMOS D-latch will be, we have compared it to an ordinary static CMOS D-latch and a D-latch based on mirrored gate.

The simulated D-latch topology used in this work can basically be seen in the schematic of Fig. 3b. That is the topology for the FGMOS D-latch. The static CMOS and mirrored gate are also similar to the design in Fig. 3b but they have no buffers on the output.

When we have the D-latch characterized together with all the previous simulated basic digital elements we will be able to create all kinds of digital systems in subthreshold FGMOS both finite state machines and combinatorial logic systems.

The basic building block we have been used for the FGMOS digital gates are the Majority-3 gate seen in Fig. 2.a

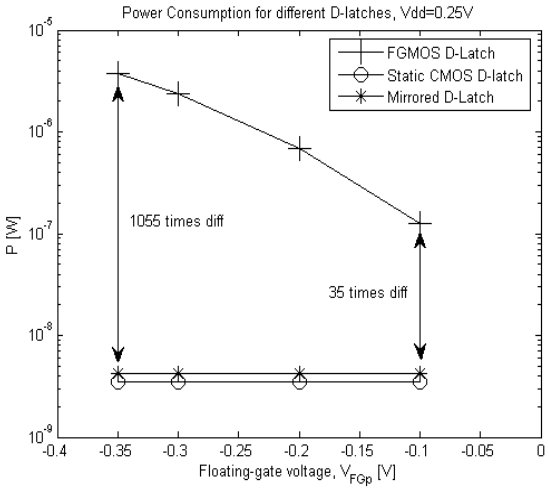

Fig. 4. Power consumption for the simulated D-latches

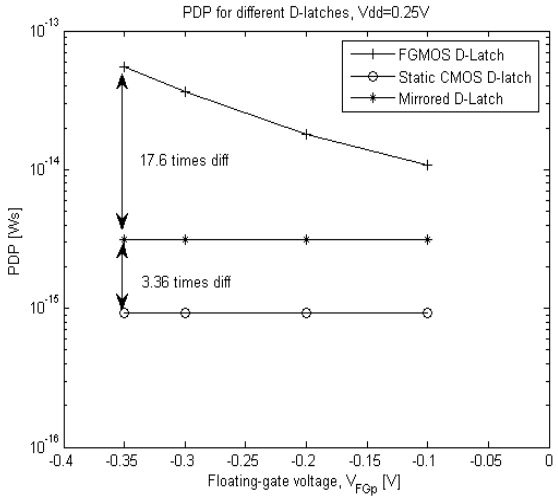

Fig. 5. PDP performance for the different D-latches and different V_{FGp}

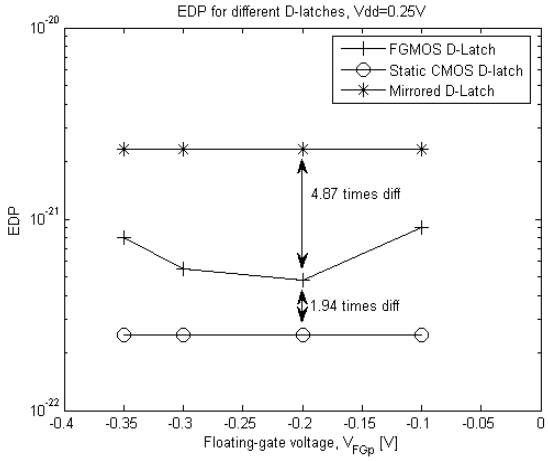

Fig. 6. EDP performance for different D-latches at different V_{FGp}

and the 3-input mirrored gate element seen in Fig. 2.b have been used for the mirrored gate designs.

IV. SIMULATIONS AND RESULTS

Our simulations in Cadence using the Spectre simulator. The process is 120 nm CMOS with low-leakage transistors.

The threshold voltage, V_{th}, for these low-leakage transistors are 383 mV for NMOS and -368 mV for PMOS. Previous work in this area, using a fixed, ideal C_{FG} suggests that the best Energy-Delay Product (EDP) performance will be obtained at 250 mV power supply when the fan-in of the circuit is not more than 3 [10]. For this reason we have chosen the power supply to be 250 mV during our simulations.

EDP is calculated from the average power consumption and the square of the minimum possible switching time for the circuit. This is the time required to still have the D-latch working properly. Each pulse is chosen 2 times the output 90% settling time, t_s and the switching period will then be 4 times t_s.

The most interesting parameters from the simulations of the latches are maximum frequency, power consumption, Power-Delay Product (PDP) and EDP. Previously Comparisons of flip-flops and latches [11] have also been considered when we have done the comparisons and the simulations have all been performed with worst case input stimuli to make the comparisons as equal as possible.

The simulations show that for power consumption and PDP, the design with ordinary static CMOS without doubt has the best performance. In the simulated interval for V_{FG}, the CMOS latch has between 35 and up to over 1000 times lower power consumption than the FGMOS latch. This can be seen in Fig. 4. For the D-latch based on the mirrored gate there are almost no difference compared to static CMOS. When it comes to the PDP, see Fig. 5, the difference between the simulated d-latches are not as large as for Power consumption. At most, the PDP is about 60 times better for CMOS than for FGMOS and 3.3 times better than the Mirrored gate D-latch.

Two of the most important performance parameters are the EDP and maximum switching frequency for the circuits. Since these simulations have been performed in subthreshold the maximum switching frequency and EDP will vary very much with different configurations.

From Fig. 6 we can see the EDP performance curve for the simulated circuits. It show us that the FGMOS D-latch design has a local minimum EDP somwhere around a V_{FGp} = 250 mV and FGMOS will at no point be better with respect to lower EDP compared to static CMOS.

In best case our simulations shows, EDP is around 2 times higher for FGMOS compared to static CMOS and the Mirrored Gate based D-latch will be around 9 times higher.

The maximum switching speed for all the D-latch circuits

Vdd = 0.25 V	Max Freq. [Hz]	Compared to CMOS
Static CMOS	$3.79*10^6$	1
Mirrored Gate	$1.35*10^6$	0.356
FG (V_{FGp}=0.10V)	$1.18*10^7$	3.11
FG (V_{FGp}=0.20V)	$3.79*10^7$	10
FG (V_{FGp}=0.30V)	$6.58*10^7$	17.36
FG (V_{FGp}=0.35V)	$6.85*10^7$	18.07

Table 1. Maximum Frequency Comparison for the different D-latches

can be seen in Table 1. It shows that switching speed is best for the FGMOS circuits with a maximum of 18 times higher speed than for static CMOS. The mirrored gate D-latch has the slowest switching speed with only 36% of the CMOS switching speed.

V. CONCLUSIONS

In this paper we have presented simulation results from floating-gate circuits with fan-in 3 that has been used to design a D-latch. The circuit has been compared with simulations of a D-latch based on static CMOS and on mirrored gate elements. The simulations have been performed in subthreshold with a power supply of 250 mV.

The simulations show that CMOS will have clearly better performance in terms of PDP (up to 60 times) and power consumption (up to 1000 times) compared to it's competitors. When it comes to EDP the advantage for CMOS is only about 2 times better performance and the possibility to design better D-latches in FGMOS with other sizes and topologies can not be excluded.

The best argument for using FGMOS D-latch compared to CMOS or mirrored designs in subthreshold is that FGMOS will have significantly higher speed than both of the others. Our simulations indicate that up to 18 times faster switching speed and a maximum speed of 68.5 MHz is possible when using FGMOS.

The high improvement of switching frequency our simulations shows for FGMOS compared to CMOS comes at a price of increased power consumption with up to three orders of magnitude. This big difference in power consumption is mainly caused by the reason that the FGMOS circuits will be completely turned on by the floating-gate voltages since they are higher than the threshold voltages in those cases. When it comes to the mirrored gate D-latch, we have found no advantages for using instead of CMOS or FGMOS at subthreshold power supply.

VI.REFERENCES

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