Basic Speed and Power Properties of Digital Floating-Gate Circuits Operating in Subthreshold

Jon Alfredsson[1], Snorre Aunet[2] and Bengt Oelmann[1]

[1]Department of Information Technology and Media,
Mid Sweden University, SE-851 70 Sundsvall, SWEDEN.
E-mail: Jon.Alfredsson@miun.se, Bengt.Oelmann@miun.se

[2]Department of informatics, University of Oslo, Norway.
E-mail: Snorre.Aunet@ifi.uio.no

Abstract

For digital circuits with ultra-low power consumption, floating-gate circuits have been considered to be a technique potentially better than standard static CMOS circuits. By having a DC offset on the floating gates, the effective threshold voltage of the floating-gate transistor is adjusted and the speed and power performance can be altered. In this paper the basic performance related properties such as power, delay, power-delay product (PDP), and energy-delay product (EDP) for floating-gate circuits operating in subthreshold are investigated. Based on circuit simulations in a 120nm process technology, it is shown that for the best case, the power can be reduced approximately by one order of magnitude at the expense of increased delay, while the PDP is more or less constant in comparison to static CMOS. The EDP can be reduced by two orders of magnitude at the expense of reduced noise margins.

1. Introduction

Circuits that have very low power consumption without too much loss in speed will always be of high interest for circuit designers. With today's increasing demand for portable applications with long lasting battery lifetime the need for such circuits are higher than ever before. By reducing the power supply below the circuit's threshold voltage, into the subthreshold region, the power consumption can be reduced several orders of magnitude compared to circuits operating in strong inversion [1],[2].

This reduction in power supply also reduces the maximum circuit speed. To increase the speed and still have very low power consumption floating-gate MOS (FGMOS) technique has been proposed.

FGMOS circuits are a circuit design technique that is very suitable for low-power applications [3],[6]. It can be made in a standard CMOS process where an extra floating-gate capacitance is introduced on the gate node. This floating-gate capacitance shifts the threshold voltage of the MOS-transistor so that the needed effective threshold voltage on the gate is changed. The shift is controlled by a charge deposited on the floating-gate node [3].

Ideally, the floating-gate has no DC path to other nodes but in reality there are gate leakage current that discharge the node within a certain amount of time. This is an increasing problem when the gate oxide gets thinner and there exists methods to handle this, i.e.[4],[5]. In this work the floating-gate voltages are assumed to be constants.

When it comes to circuit's performance in subthreshold region, some commonly used figure of merits for comparison are power consumption (P), power-delay product (PDP) and energy-delay product (EDP) [6],[7]. The power consumption alone is not good enough to use since just lowering the speed will reduce it. For circuits where speed is of less importance both PDP can be used for comparison but the best figure when speed performance is critical is EDP [7],[8].

The aim of this work has been to find out the basic speed and power related properties of floating-gate circuits operating in subthreshold.

In this paper we present simulation results from a comparison between the standard static CMOS and FGMOS circuit techniques at different subthreshold power supplies. The FGMOS circuits have been simulated for different floating-gate voltages and we shows that for the best cases the power consumption and EDP is much lower than for an equal CMOS circuit while PDP is almost equal. The main costs to achieve these performance improvements are lower noise margins and higher leakage and switching currents.

2. FGMOS circuits

Floating-Gate MOS transistors are basically normal MOS-transistors with a shifted threshold potential. The shifts in the threshold potential are made by introducing a node voltage on an extra gate capacitance in series with the normal gate capacitance [3]. It is called a floating-gate capacitance (C_{FG}) and is in series with the transistor's gate

node. Programming of the FGMOS introduces a charge on it, This will shift the threshold voltage and the transistor's gate is said to be floating. A floating-gate transistor and inverter are shown in figure 1a and figure 1c. Figure 1b shows the normal static CMOS inverter.

Depending on how large the floating-gate voltage (V_{FG}) is, the applied node voltage needed to get the transistor into strong inversion region will be different. V_{FG} is determined during the design process and its purpose is to reduce the transistors needed gate-source voltage, V_{gs}. The floating-gate circuits are then programmed with the selected V_{FG} once and then they should be fixed.

To keep the floating-gate voltage constant, it is needed to have no charge leakage from the floating-gate node. Ideally this is the case. In reality some kind of refresh circuitry must be introduced to keep the charge [4],[5].

Applying a V_{FG} on the floating-gate node will not only shift the threshold voltage for the transistor but also shift the transistor's on- and off currents. When the transistors are working they will have different leakage drain-source current compared to normal static CMOS circuits.

The gate potential of floating-gate circuits can be implemented by several different methods. One example is UV-activated conductance between the gate and source that enables programming of the FGMOS circuit. Other methods that can be used are Fowler-Nordheim tunneling and hot-electron injection [9],[10].

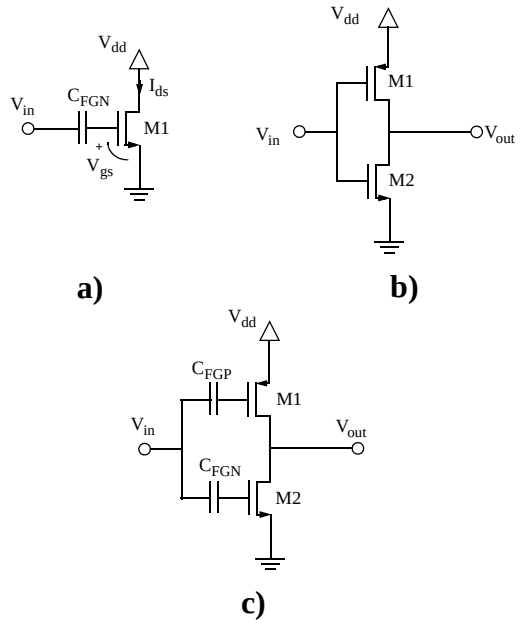

Fig. 1. a) Floating-gate nMOS transistor
b) CMOS Inverter
c) FGMOS Inverter

3. Circuit characterization method

When a circuits power supply is scaled down to the subthreshold region, the power consumption and speed for the circuit will be very much reduced. This is a well known phenomenon for the weak inversion region and there have been several papers published on power supply scaling and subthreshold circuits [1],[6],[7],[11],[12].

In this research we have been doing almost all simulations in the subhtreshold region. By using FGMOS technique to shift the threshold of the transistors we can achieve better speed and performance, more similar to the performance of a transistor in strong inversion.

The simulations have been performed with ideal floating-gate capacitances, C_{FG}, (without parasitic effects i.e. from the capacitor plates) so the results presented here is in that way the best achievable. The charge leakage from the floating-gate nodes has not either been taken into account, but this can be handled by external circuitry.

Both CMOS inverters as well as single transistors (nMOS and pMOS) have been compared to floating-gate circuits (FGMOS inverter, FGnMOS and FGpMOS) in this work. All the compared transistors have the same length and width in order to be as similar as possible. They have been compared with respect to static on and off (leakage) currents at different floating-gate voltages to get an overview of how it varies.

The on (dynamic) and off (static) currents for a MOS inverter can also define the noise margin, NM, for digital circuits. The following expression should then be used, I_{ds} is the drain-source current of the inverter [6].

$$NM = \frac{I_{on}}{I_{off}} = \frac{I_{ds}^{max}}{I_{ds}^{min}} \qquad (1)$$

With the simulated currents from the transient analysis we have calculated the NM at different power supply for the inverters in our study.

Both static CMOS and FGMOS inverters have been designed to be able to make comparisons from the transient analyses, see figure 1b and figure 1c. They have the same transistor sizes to be as comparable as possible. To get symmetric switching for the inverters, (the output signal, V_{out}, should be $V_{dd}/2$ exactly when the input signal, V_{in}, is equal to $V_{dd}/2$,) the CMOS inverter is tuned by selecting the transistor widths. The FGMOS inverter also needs to be balanced for each different floating-gate voltage to reach the symmetric switching.

To balance the FGMOS inverter, the initial floating-gate voltages, V_{FG}, for the FGnMOS and FGpMOS transistors in the FGMOS inverter needs to be determined. These voltages are calculated from a balancing circuit proposed in [13]. It has an OP-amplifier connected in a feedback loop to determine one of the floating-gate voltages when the other one is a fixed value. With this balancing circuit, the voltage transfer characteristic (VTC) are set so that a V_{in} of $V_{dd}/2$ will generate a V_{out} of $V_{dd}/2$.

The balanced inverters have been connected to 3-stage ring oscillators in order to perform the transient analysis simulations. The average current and gate delay, i_{avg} and t_p, has been observed for an inverter in the ring oscillator. For simulations, i_{avg} and t_p are independent of how many inverter stages the ring oscillator has. Number of stages is only important for real physical implementations.

Two commonly used figures of merit to compare cir-

cuits with low-power and high-speed are the power-delay product (PDP) and the energy-delay product (EDP) [2],[7] (see equation (2) - (4)). When performance is a critical parameter the EDP is a much better figure to use for comparison than the PDP. The PDP is an energy-only figure of merit and therefore only good to use when speed performance does not matter [7]. From an energy point of view the PDP will always be equal or higher for FGMOS than for CMOS when a V_{FG} is applied that lower the needed threshold voltage. Higher PDP and larger leakage current is the price we have to pay to achieve better speed performance for FGMOS at subthreshold voltage supply.

While PDP is an energy measure only, the EDP is a better figure to use when speed is important because it is a weighted measure of the consumed energy multiplied by the cycle time when its consumed, see eq.(4).

The EDP is calculated as the PDP times the signal propagation delay

$$Power = I_{avg} \cdot V_{dd} \tag{2}$$

$$PDP = Power \cdot t_p = I_{avg} \cdot V_{dd} \cdot t_p \tag{3}$$

$$EDP = V_{dd} I_{avg} t_p \cdot t_p = PDP \cdot t_p \tag{4}$$

where I_{avg} is the average switching current and t_p is the inverter's minimum propagation delay [7],[8].

In floating-gate transistors, the floating-gate capacitance (C_{FG}) is added in series with the normal gate capacitance (including parasitics), C_g, and the input signal will then be reduced in amplitude. The amount of reduction is depending on how large the floating-gate capacitances are. The effective signal on the transistor's gate (V_{eff}) can be calculated from V_{in} with this formula [9]:

$$V_{eff} = V_{in} \cdot \frac{C_{FG}}{C_{FG} + C_g} \tag{5}$$

4. Simulations and results

Our simulations have been performed in Cadence with the Spectre simulator in a 120nm CMOS process technology. The transistors are of low-leakage type and the sizes have been the same for both the CMOS and FGMOS designs. Minimum gate lengths (120nm effective length) and a width of 150nm for NMOS and 380nm for the PMOS have been used. With these sizes, the transistors' normal C_g has been calculated from simulations to be about 0.1fF for nMOS and 0.3fF for pMOS.

To maintain enough amount of the input signal in our simulations, the total C_{FG} for the FGMOS inverters has been chosen to be 8 times larger than C_g. This will get an effective V_{in} of more than 88% of the original signal.

The threshold voltage, V_{th}, for these low-leakage transistors are around 370mV. The simulations of FGMOS and CMOS inverters have been performed with a power

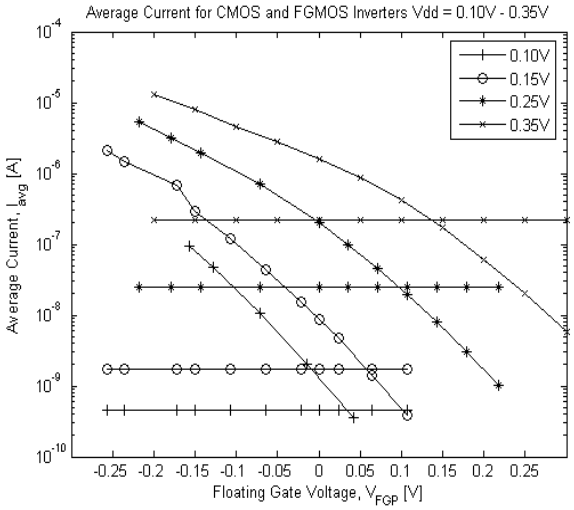

Fig. 2. Average Inverter Current for CMOS and FGMOS at different power supply and floating-gate voltages.

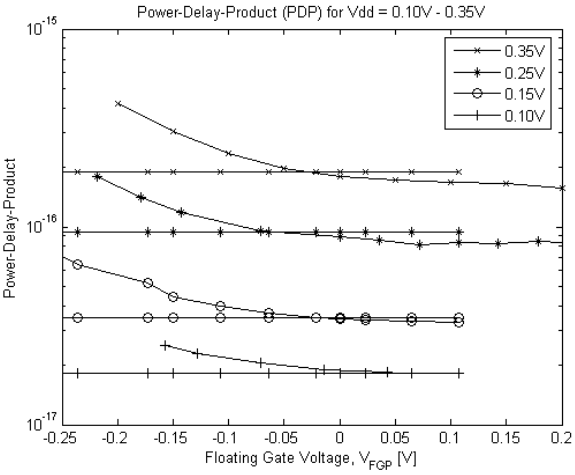

Fig. 3. PDP for CMOS and FGMOS inverters at different power supply and floating-gate voltages.

supply below threshold voltage. The chosen power supply voltages for our simulations are 100mV, 150mV, 250mV and 350mV. The CMOS circuit has also been simulated with a power supply of 1.20V to compare the speed and current in a normal case of strong inversion.

Figure 2 shows the drain current for CMOS and FGMOS inverters at different V_{dd} when V_{FGP} varies. The straight horizontal lines are for CMOS that are independent of V_{FGP}. For some V_{FGP}, a current (and power) reduction of 10 times is possible for FGMOS.

The PDP is plotted in figure 3 and it is almost equal to CMOS and approximately constant for each subtreshold power supply and positive V_{FGP}.

Figure 4 is a similar plot like the one in figure 2 but instead it is the propagation gate delay that is plotted for different V_{dd} and V_{FGP}. Just like figure 2, the plotted lines for the CMOS inverter are constant and independent of the V_{FGP}.

When it comes to the EDP for the FGMOS and CMOS inverters they are plotted in figure 5. The plot shows that it is possible to achieve much better EDP for FGMOS compared to static CMOS if the floating-gate voltage are chosen in certain ways. It will be possible to achieve an

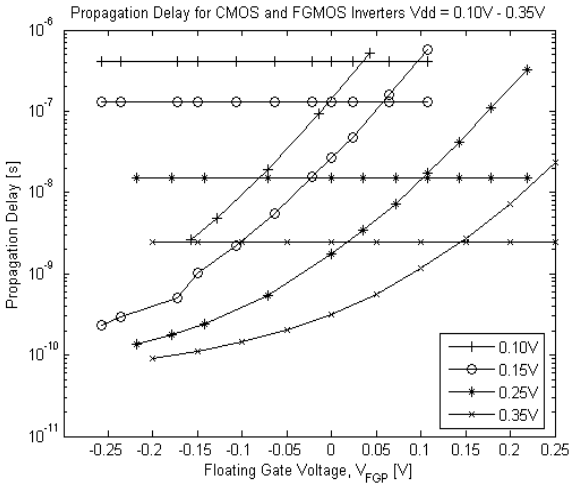

Fig. 4. Propagation Delay for CMOS and FGMOS inverters at different power supplt and floating-gate voltages.

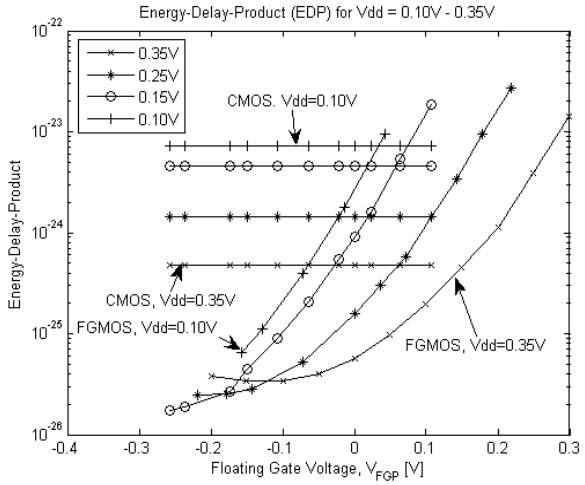

Fig. 5. EDP for CMOS and FGMOS inverters at diffrent power supply.

EDP that is 260 times lower for FGMOS than for CMOS at 150mV power supply when V_{FGP} are around -200mV.

Even when the power supply is reduced to 100mV, a reduction in the EDP of more than 100 times is possible to get. That is more than two orders of magnitude.

The Noise Margin, NM, will naturally become smaller and smaller when power supply is reduced. Also it will vary with the floating-gate potential. The better EDP we want to have, the smaller NM we need to accept. That is a trade-off price we have to pay. How the NM varies with V_{dd} and V_{FGP} can be seen in figure 6.

5. Conclusions

In this paper, we have presented a comparison of CMOS and FGMOS circuits with respect to the power, PDP and EDP when the power supply is below subthreshold voltage of the transistors.

In the best case for FGMOS inverters, the power consumption can be reduced by more than one order of magnitude and EDP can be reduced by more than two orders of magnitude compared to CMOS. Thc cost to achieve this reduction in EDP is mainly a reduction in the circuits

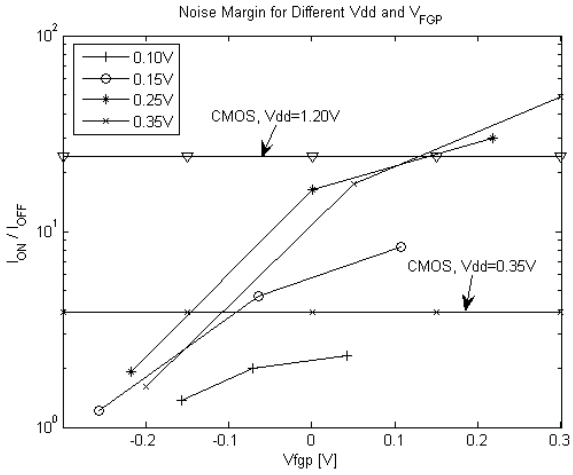

Fig. 6. Noise Margin, NM, for Different power supply and V_{FGP}.

noise margin.

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