Analysis and Design of a New Extendable Sepic Converter with High Voltage Gain and Reduced Components for Photovoltaic Applications

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Abstract - **In photovoltaic applications, a DC-DC converter is required to increase the output voltage of the photovoltaic system. In this paper, a new extended SEPIC converter with the capability of high voltage gain for photovoltaic applications is introduced. The proposed topology includes an extended switched-capacitor converter along with one SEPIC converter. The extended switched-capacitor converter operates with a constant conversion gain while the SEPIC converter is controlled by the Duty Cycle to extract maximum power from PV panel. Reduction of the number of power switches and capacitors are the most advantages of the proposed topology. Also, the input current of proposed topology is continuous which is suitable for PV applications. Finally, the performance of the proposed converter is verified by simulating in the PSCAD/EMTDC simulation software.**

Index Terms - SEPIC converter; Switched-capacitor; High voltage gain; Photovoltaic applications.

I. INTRODUCTION

The application of clean and renewable energy, such as photovoltaic (PV) systems has been a focus in academia and industry over the last decade [1-3]. Increasing in prices and the limited amount of non-renewable energy sources has led to the use of renewable energy sources. PV systems use the solar energy to generate electricity. However, the generated DC voltage by a PV system is very low. To solve this problem, DC-DC converters are used in renewable energy sources [4-7].

To achieve high voltage gains, several DC-DC converters have been proposed in PV systems. Classical boost and buck-boost converters require large duty ratios. The maximum voltage gain that can be achieved is constrained by the parasitic resistive components in the circuit and the efficiency is drastically reduced for large duty ratios. There are diode reverse recovery problems because the diode conducts for a short period of time [8]. Typically, high frequency transformers or coupled inductors are used to achieve high voltage conversion ratios [9-18]. But, the transformer design is complicated and leakage inductances increase for achieving larger gains, as it requires bigger number of winding turns. This leads to voltage spikes across the switches and voltage clamping techniques are required to limit voltage stresses on the switches. Consequently, it makes the design complicated.

To overcome these limitations, diverse DC-DC converters such as the interleaved boost converters [19, 20], soft switching boost converters [21] and voltage multiplier converters [22, 23] have been proposed which can provide larger voltage gain than conventional DC-DC converters. It is obvious that other types of high voltage gain converters are based on the combination of these structures have been proposed recently [24-28]. Each one of these structures has advantages and disadvantages.

One of the most important types of high voltage gain converters is voltage multiplier converters. These topologies have fixed input and output voltage ratio. The main benefits of the voltage multiplier converters are low weight, small size, high power density and high efficiency. However, the achieved voltage gain is fixed but the output voltage cannot be regulated because of depending on the input voltage. Moreover, due to use of a large number of power switches in these structures, the costs and circuit size are increased.

In this paper, a new extended SEPIC (Single-Ended Primary Inductor Converter) converter with high voltage gain is proposed to solve above mentioned limitations. The proposed dc-dc converter which uses minimum number of components and its input current is continuous. The operation modes, power losses, comparative studies, and simulation works are illustrated in depth.

II. CIRCUIT DISCRIPTION

A. Proposed topology configuration

In the switched-capacitor converters, the energy transferred by the capacitors. By the high-frequency switching actions, the capacitors will be connected in series or in parallel directly by the switches. By considering to this point, in this paper, the proposed topology has been combined from an extended switched-capacitor and a SEPIC converter. Fig. 1 shows the studied topology which includes two stages. The first stage is an extended switched-capacitor converter and the second one is a SEPIC converter. First stage consists of m capacitors (C_1,

C_2, … , C_m), m+1 power switches S_1, S_2, … , S_m, S_t, 2m power diodes (D_{x1}, $D_{x2, \dots}$, D_{xm}, D_{y1}, D_{y2}, … , D_{ym}) and a dc voltage source (V_{in}). Moreover, the SEPIC converter is composed of a switch (S), two inductors (L_1, L_2), two capacitors (C_S, C_O), a diode (D_O) and a resistive load (R_L). Based on Fig. 1, the input voltage of the converter is a PV source. Therefore, the output voltage of PV is always low. This converter can be effective to overcome some limitations like following problems:

- Discontinuous input current.
- Limited voltage gain
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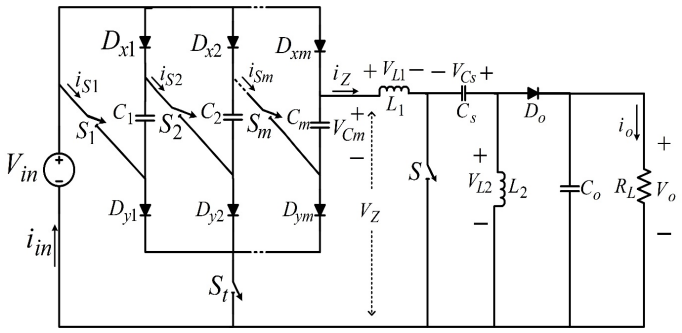


Fig. 1: The proposed topology.

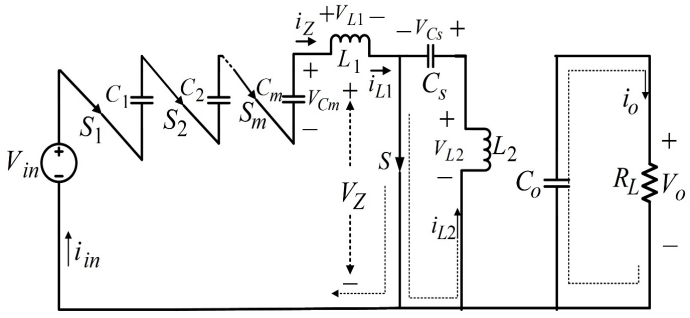
B. *Switching states analysis*

For the theoretical analysis, it is assume that all switches, diodes, inductors and capacitors are ideal. The proposed converter has two operating modes during each switching period. The corresponding equivalent circuits and the key waveforms are shown in Fig. 2 and Fig. 3 respectively.

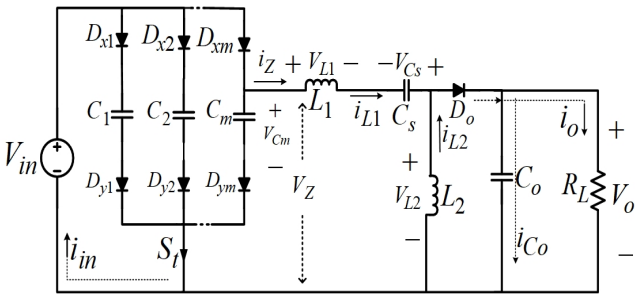
Mode 1: [0<t<DT]: The equivalent circuit of this mode is shown in Fig. 2(a). The instant t=0 is the starting time point of this subinterval, all power switches S_1, S_2, … ,S_m and S are turned on while the diodes D_{x1}, D_{x2}, … , D_{xm}, D_{y1}, D_{y2}, … , $D_{ym,}$ D_O and S_t are turned off so the inductors L_1 and L_2 are charged. The voltage across C_S is equaled V_z. C_O provides required energy of the load. Therefore, the voltage V_z is obtained as:

$$V_Z = V_{in} + V_{C_1} + V_{C_2} + \dots + V_{C_m} \quad (1)$$

Mode 2: [DT<t<T]: The equivalent circuit of this mode is shown in Fig. 2(b). At t=DT, S_1, S_2, … ,S_m and S are turned off and the switch S_t and the diodes D_{x1}, D_{x2},…, D_{xm}, D_{y1}, D_{y2}, … , $D_{ym,}$ D_O are turned on. Then, the capacitors C_1, C_2,…,C_m will be parallel and they are charged by voltage V_{in}. Also, C_S, C_O and L_1, L_2 are charged and discharged, respectively.



(a)



(b)

Fig. 2: Switching modes of the proposed converter, (a) Mode 1, (b) Mode 2.

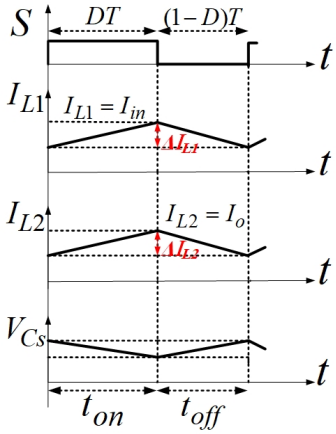


Fig. 3: Key waveforms of the proposed converter.

C. *Voltage gain*

To obtain the voltage gain we have to use operating modes in this paper because it is a most important parameters in a boost DC-DC converter and it should be high in order to large efficiency and low losses.

It is obvious that the average voltage of inductors L_1 and L_2 at the beginning and the ending are zero. Then,

$$\int_0^T V_{L_1} dt = \int_0^{DT} V_Z dt + \int_{DT}^T -V_O dt = 0 \quad (2)$$

By solving (2), we will have:

$$V_O(1-D) = DV_Z \quad (3)$$

Thus, V_O will be obtained as following:

$$V_O = \frac{D}{1-D} V_Z \quad (4)$$

As considered to Fig.1, V_z is the output voltage of extended switched-capacitor converter which is

$$V_Z = (m+1)V_{in} \quad (5)$$

Where m is the number of capacitors C_1,…, C_m. By using (4), (5), the voltage gain of proposed topology is calculated as:

$$V_o = \frac{D}{1-D}(m+1)V_{in} \quad (6)$$

Where, D is the duty cycle of switch S.

III. PARAMETERS DESIGN

To calculate the most significant parameters of the proposed converter, using from switching modes in Fig. 2 and the key

waveforms in Fig. 3 is inevitable. The values of components such as inductors, capacitors, and total voltage rating of the switches are calculated in this section.

A. The values of inductors

In this section, the magnitudes of L_1 and L_2 are computed. The inductors L_1 and L_2 are charged in first mode and discharged in second one. Therefore, they can be obtained as:

$$V_Z = V_{L_{1on}} = L_1 \frac{dI_{L_1}}{dt} = L_1 \frac{\Delta I_{L_1}}{t_{on}} \tag{7}$$

$$V_Z . t_{on} = L_1 \Delta I_{L_1} \tag{8}$$

$$t_{on} = DT \tag{9}$$

Where, $T = \frac{1}{f_s}$ is one switching cycle, and t_{on} is the time in first mode.

$$V_Z . DT = L_1 \Delta I_{L_1} \tag{10}$$

The current ripple of inductor L_1 is computed by:

$$\Delta I_{L_1} = \frac{V_Z D}{L_1 f_s} \tag{11}$$

Then, the inductor L_1 is obtained.

$$L_1 = \frac{V_Z D}{\Delta I_{L_1} f_s} \tag{12}$$

Similarly, ΔI_{L2} and L_2 are equaled by:

$$V_O = V_{L_{2off}} = L_2 \frac{di_{L_2}}{dt} = L_2 \frac{\Delta I_{L_2}}{t_{off}} \tag{13}$$

$$t_{off} = (1-D)T \tag{14}$$

Then,

$$\Delta I_{L_2} = \frac{(1-D)V_O}{L_2 f_s} \tag{15}$$

$$L_2 = \frac{(1-D)V_O}{\Delta I_{L_2} f_s} \tag{16}$$

B. The values of capacitors

To obtain the values of capacitors C_1, …, C_m, it is evident that these capacitors are in series in first mode and in parallel in the second mode. Based on Fig. 2(a), the current flowing through these capacitors are the same. It means:

$$i_{C_1} = i_{C_2} = \cdots = i_{C_m} = -i_z = -\frac{I_O}{1-D} \tag{17}$$

Moreover, according to Fig. 2(b), the voltage across capacitors is equaled by:

$$V_{C_1} = V_{C_2} = \cdots = V_{C_m} = \frac{1}{C_m}\int_0^{DT} i_{C_m} dt + V_{C_m}(0) = \frac{1}{C_m}\int_0^{DT} \frac{I_O}{1-D} dt + V_{C_m}(0) \tag{18}$$

The output current I_O, according to the Ohm law equals:

$$I_O = \frac{V_O}{R_L} \tag{19}$$

By using (18) and (19) the values of voltage ripple of capacitors are obtained as follows:

$$\Delta V_{C_1} = \Delta V_{C_2} = \cdots = \Delta V_{C_m} = \frac{DV_O}{(1-D)C_m f_s R_L} \tag{20}$$

Then, the values of capacitors by utilizing (20) are computed.

$$C_1 = C_2 = \cdots = C_m = \frac{DV_O}{(1-D)\Delta V_{C_m} f_s R_L} \tag{21}$$

Considering the ideal elements, the input current of the proposed structure (I_{in}) can be expressed as:

$$I_{in} = \frac{(m+1)D}{1-D} I_O \tag{22}$$

C. Total voltage rating of switches

Total voltage rating of the switches (TVRS) is a significant parameter in a power electronic converter. Reduction of the TVRS will be led to reduction of costs. The sum of the voltage rating of switches S_1, …, S_m which is V_{Si} equals:

$$\sum_{i=1}^{m} V_{S_i} = mV_{in} \tag{23}$$

The voltage rating of the switch S_t (V_{St}) is calculated by:

$$V_{S_t} = mV_{in} \tag{24}$$

Moreover, the voltage rating of the SEPIC converter S (V_S) is expressed as:

$$V_S = \frac{(m+1)D}{1-D} V_{in} \tag{25}$$

By using (23)-(26), the TVRS of the proposed topology can be obtained as:

$$TVRS = V_{S_i} + V_{S_t} + V_S = (2m + \frac{(m+1)D}{1-D})V_{in} \tag{26}$$

IV. POWER LOSSES

In the proposed converter, each switch has two types of losses which are called conduction and switching losses. Meanwhile, there are some other losses in the switches like capacitance and diode losses. However, the value of them is negligible and less than conduction and switching losses. Thus, in this section, these two losses (conduction and switching losses) are calculated. Generally, the conduction loss of a switch is determined by the voltage of it.

$$P_{Cond} = V_{on} I_{ave} + R_s I_s^2 \tag{27}$$

Where V_{on}, R_s, I_{ave} and I_s represent the on-state voltage of the switch, the equivalent resistance during on-state of the switch, the average and RMS current of the switch, respectively. The conduction losses of the switches in proposed topology are included the conduction losses of switches S_1,…,S_m ($\sum_{i=1}^{m} P_{Cond,S_i}$), the switch S_t ($P_{Cond,St}$) and the switch S ($P_{Cond,S}$). Thus, we have:

$$P_{Cond} = \sum_{i=1}^{m} P_{Cond,S_i} + P_{Cond,S_t} + P_{Cond,S} \quad (28)$$

By using operating modes and their analysis, the values of three above conduction losses can be expressed as:

$$\sum_{i=1}^{m} P_{Cond,S_i} = \frac{mV_{on,S_i}.DI_O}{1-D} + \frac{mR_{s,S_i}.DI_O}{(1-D)^2} \quad (29)$$

$$P_{Cond,S_t} = \frac{mV_{on,S_t}.DI_O}{1-D} + \frac{m^2R_{s,S_t}.D^2{I_O}^2}{(1-D)^3} \quad (30)$$

$$P_{Cond,S} = \frac{V_{on,S}DI_O}{1-D} + \frac{R_{s,S}.DI_O{}^2}{(1-D)^2} \quad (31)$$

To obtain switching losses of the proposed converter, the values of voltage rating of the switches are required. Totally, in a specific switch, the switching losses is calculated as:

$$P_{sw} = f_s(\int_0^{t_{on}} V_sI_sdt + \int_0^{t_{off}} V_sI_sdt) \quad (32)$$

Where V_s and I_s represent the voltage of a switch and flowing current of that in two operating modes. The total switching losses in proposed structure (P_{sw}), is obtained by:

$$P_{sw} = \sum_{i=1}^{m} P_{sw,S_i} + P_{sw,S_t} + P_{sw,S} \quad (33)$$

Where they are switching losses of the switches S_i, S_t and S, respectively. These parameters are equaled as:

$$\sum_{i=1}^{m} P_{sw,S_i} = \frac{f_sV_{in}V_O}{6R_L(1-D)}(t_{on} + t_{off}) \quad (34)$$

$$P_{sw,S_t} = \frac{m^2f_sV_{in}V_OD}{6R_L(1-D)^2}(t_{on} + t_{off}) \quad (35)$$

$$P_{sw,S} = \frac{(m+1)f_sV_{in}V_OD}{6R_L(1-D)^2}(t_{on} + t_{off}) \quad (36)$$

Hence, the total losses of the proposed converter (P_{Loss}) are sum of the conduction and switching losses as follows:

$$P_{Loss} = P_{Cond} + P_{sw} \quad (37)$$

V. COMPARISON STUDIES.

In order to make the analysis clear and to clarify the feature of the proposed converter (advantages and disadvantages), some comparisons are discussed here. The number of used switches, voltage gain and other features are compared in Table. I. According to this comparison list, it is clear that the input current of proposed topology is continuous. Nevertheless, in the other topologies, it is discontinuous. Meanwhile, the number of used switches and the TVRS in proposed converter is less than the others which it is led to reduction of cost. Because, in a power converter, the cost is related to the number of utilized switches and voltage rating of switches. This advantage is caused light weight and easy control.

Table I. Comparison of some multiplier converters.

Type of topology	[24]	[25]	Proposed converter
Number of capacitors	M	m+1	m
Number of switches	3m	2m	m+1
Cost	High	Average	Low
Voltage gain	$(m+1)V_{in}$	mV_{in}	$\frac{(m+1)D}{1-D}V_{in}$
TVRS	$(4m-4)V_{in}$	$2mV_{in}$	$(2m+\frac{(m+1)D}{1-D})V_{in}$
Output voltage	Constant	Constant	Variable
Input current	Discontinuous	Discontinuous	Continuous
MPPT regulation	No	No	Yes

Capability of voltage regulation is a significant feature that only the proposed structure can be set the output voltage by using duty cycle of switches in each voltage level and tracking maximum power point of PV panels.

Moreover, the number of utilized charging capacitors in proposed converter and the introduced topology in [24] are the same, but it is less than the suggested topology in [25].

The output voltage in proposed structures in [24], [25] is constant. However, in presented topology of this paper is different. Based on these descriptions, the proposed structure has better performance than the others and all above explanations prove this fact.

VI. SIMULATION RESULTS

To verify the analytical results, the proposed converter has been simulated for m=3 in *PSCAD*. Fig. 4 indicates the simulated circuit. It is clear that in the simulated topology all employed components have been selected with suitable values in order to transfer energy to the output side with high efficiency and low losses. The converter is designed to operate with PV systems. The values of the utilized components in simulation are listed in Table II.

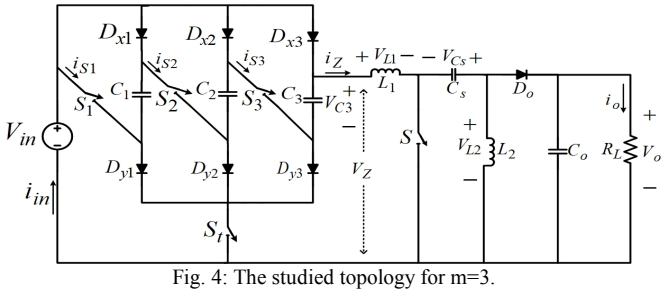


Fig. 4: The studied topology for m=3.

Fig. 5 presents the current waveforms of inductors L_1 and L_2 which shows charge and discharge periods. According to this figure, it is easy to find out the input current of proposed topology is continuous. Fig. 6 shows the output capacitor current waveform which provides the output load in first mode and is charged in second mode. Fig. 7 displays the voltage

waveform across the power switches. These waveforms specify the voltage rating of the power switches. Fig. 7(a) indicates the voltage rating of the switch S which is nearly 125V. The voltage rating of the switch S_t is presented in Fig. 7(b) which is approximately 86V. Also, the voltage rating of the switch S_1 is shown in Fig. 7(c) which is nearly 30V. Obviously, the voltage rating waveforms of the other switches are alike to this figure. As a result of these discussions, the voltage rating of switch S is bigger than the others.

Table II. Magnitudes of components of the converter.

Parameter	Magnitude
V_{in}	30V
M	3
V_o	1200V
$C_1=C_2=\cdots=C_m$	52.08 µF
C_s	1.44 µF
C_o	0.14 µF
D	0.9
L_1	0.9mH
L_2	1mH
R_L	2880 Ω
f_s	24kHz
P_o	500W
ΔI_L	5A
ΔV_C	10%

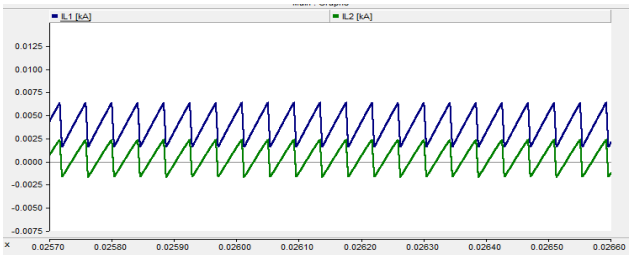


Fig. 5: Simulation waveforms of L_1 and L_2.

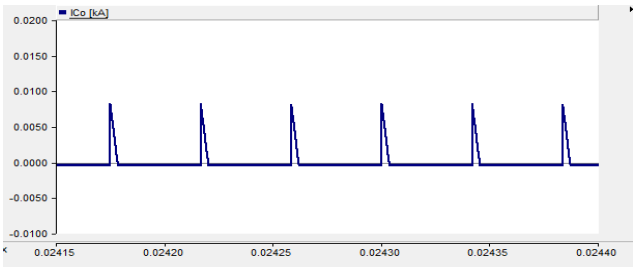
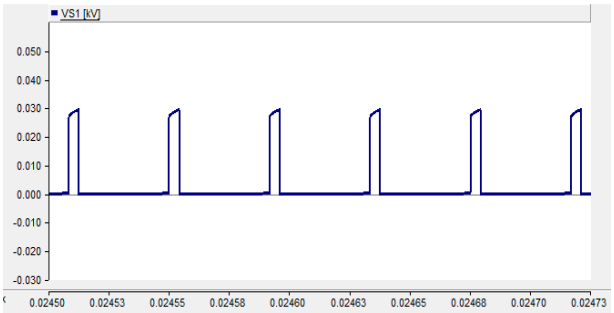
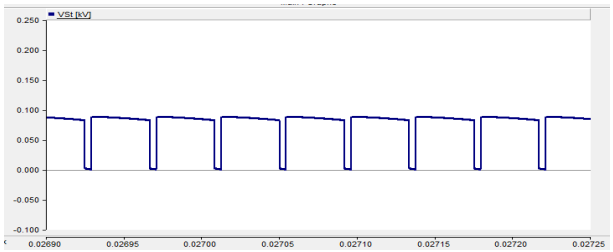


Fig. 6: Waveform of output capacitor current I_{Co}.



(a)



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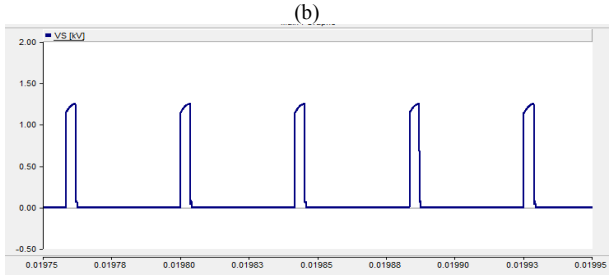
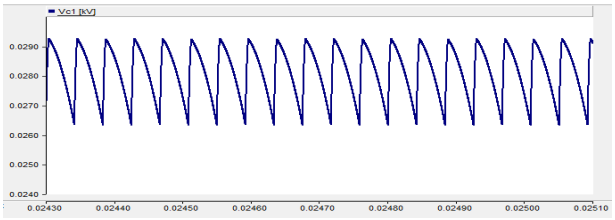


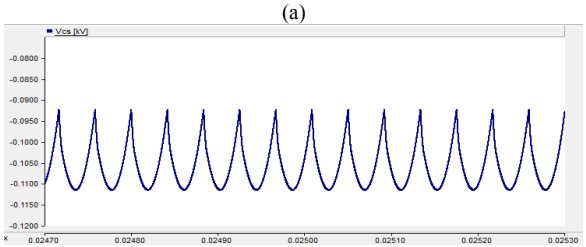
(c)

Fig. 7: The voltage rating of the switch (a) S, (b) S_t and (c) S_1.

Fig. 8 presents the waveform of the voltage across each capacitor. In Fig. 8(a), the voltage across capacitor C_1 is indicated which is same as other capacitors. Meanwhile, Fig. 8(b) displays the voltage across capacitor C_S which is 111.3V. Based on the simulation results, the efficiency of the proposed structure is %95.8. It means that some of the input power while transfer to the load side is lost that it is less than %5 in proposed topology. This efficiency in comparison with the other similar structures has improved. Therefore, this topology is suitable for renewable energy applications especially PV systems. The waveform of the output voltage is shown in Fig. 9 which is 1150V.



(a)



(b)

Fig. 8: Voltage across capacitors, (a) C_1 and (b) C_S.

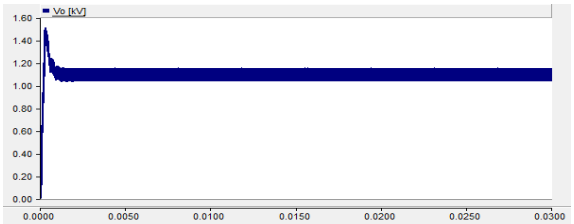


Fig. 9: The waveform of output voltage.

VII. CONCLUSION

This paper proposed a new extended SEPIC converter. Operating modes and mathematical analysis of the presented topology were analyzed. By using the proposed structure, the drawbacks of multiplier topologies were improved. The merits of this converter include: high voltage gain, continuous input current, and better regulation of output voltage. Moreover, the number of used components like power switches and charging capacitors was decreased that it is lead to easy control and low cost. These properties are shown that the proposed structure is appropriate for photovoltaic systems. Also, the simulation results confirm the performance of the presented converter.

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