

Pseudo Floating-Gate Design Limitations in Nano-CMOS with Low Power Supply

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Abstract - This paper shows simulation results from a recently proposed Pseudo Floating-Gate (PFG) technique for use in subthreshold. The design and simulations is performed in a 120 nm process CMOS technology and show that there are limitations that will make subthreshold PFG very difficult to manufacture with full functionality. The simulations show limitations in fan-in that will contribute to making it harder to manufacture structures that have small area or a high arithmetic complexity per active element. It also show bandwidth limitations for the input and output signals.

As a complement to the simulations of our PFG design we have also made a summary of several different kinds of PFG techniques that are previously developed and some of their limitations. The summary also tries to determine where the PFG techniques originates from and present an overview of the most obvious limitations they have.

I. INTRODUCTION

Reductions in power consumption are one of the most important factors for future CMOS designs according to [1]. It will not only extend the operational time for battery driven applications but it can also be beneficial for many other areas like save energy costs for the consumers and save heat removal costs for producers.

Floating-gate (FG) techniques have previously been proposed for both analog and digital designs in order to work with low voltages and has proven to be effective to reduce power consumption for signal processing circuits. [2],[3].

Signal processing circuits designed with floating-gate techniques are based on control of the effective threshold voltage seen from the driving input of a transistor. To control this effective threshold voltage, V_{th} , a charge is applied on a floating-gate node that is connected to the transistor's gate and electrically isolated from its surroundings. The charge can be applied and controlled by several different methods. Hot-electron injection has been proposed as one of those. Others are based on erasability [4], UV-reconfigurability [3] or Fowler-Nordheim (FN) tunnelling [5]. FN-tunnelling has also been proposed in combination with hot-electron injection [6]. Charging the floating-gate node will make a static shift of the effective threshold voltage and that will change the performance for the circuit.

When CMOS technologies have evolved with smaller gate lengths and reduced gate-oxide thickness, the gate-leakage through the transistor is increasing. In reality it is not

possible to create true floating-gate circuits (without leakage), and to prevent the charge from changes, the gate-oxide is preferred to have a thickness of at least 70Å [7]. If it is below that value, some kind of refresh circuits have to be used and one of the most common techniques for this is called Pseudo floating-gate (PFG).

PFGs are different techniques developed to overcome those kind of shortages with leaking transistor gates [8],[9] and PFG circuits exists in a wide variation of different styles.

With this in mind, we can see that several new PFG techniques to design floating-gate circuits have been introduced during the past years. They are all somewhat based on controlling the leaking gate charge by a large resistive connection [9],[10],[11], or eventually, by a clock switched connection to the floating-gate [12],[13],[14]. There also exists a few special PFG techniques, like for example leakage control with a diode connection. The first time a diode connection has been used to represent this large resistance in signal processing circuits is, as far as we know, in [11] and then it is called quasi floating-gate technique.(QFG)

In this paper we have aimed to design and simulate a PFG frequency doubler that also can be used as a 2-bit analog-to-digital converter (ADC). Our simulations show limitations in both design constraints and performance. The design we finally have been chosen for our circuit is a topology used in [15] which had a maximum fan-in of 3. A 2-bit ADC is a limitation since there already exist 3-bits ADC topologies in floating-gate [16], but previous work have shown that these designs require a circuit with a fan-in of 7 [18]. This high fan-in will not work in subthreshold for a typical 120 nm process according to our simulations [17]. Exploiting this 3-bits ADC with a PFG topology also showed that there are certain limitations to use PFG circuits. The PFG technique used to implement the circuit in this work is designed with a weak feedback buffer to force the FG-node to correct value.

To get an overview of other existing possible choices for PFG designs, this work also summarize the most commonly used techniques for PFG in order to find some of their major limitations and similarities. A few other studies and comparisons of floating-gate techniques are presented in [9],[19].

II. FGMOS CIRCUITS

The FGMOS (floating-gate MOS) is a technique using standard MOSFET transistors and can be fabricated in a

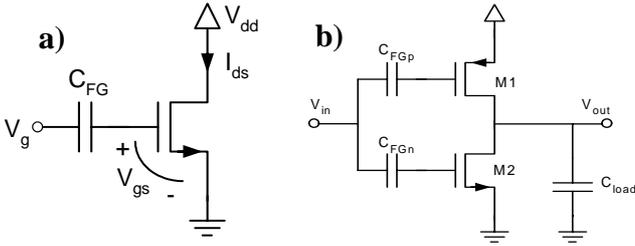


Fig. 1 a) Floating-gate nMOS transistor.
b) Ideal FGMOS inverter.

standard CMOS process with a double polySilicon layer option. The FGMOS transistors are manufactured with an extra gate capacitance in series with the normal transistor gate to create the floating-gate node. This extra capacitance connected to the gate is called a floating-gate capacitance, (C_{FG}) [20].

If the gate is completely isolated, it is called true floating-gate and if it has some leakage currents that requires recharge of the FG-node it is said to be quasi- or pseudo floating-gate (PFG). Figure 1a) shows a floating-gate transistor and figure 1b) shows a true FGMOS-inverter.

In simulations it can be easy to maintain the functionality of FGMOS circuits and still have true floating-gate but in reality it is necessary to introduce some kind of programming to re-establish the floating-gate charge on the floating-gate node and that is why the PFG techniques are introduced.

One of the easiest ways to determine proper values for the charge on the floating-gate nodes (V_{FGp} & V_{FGn}) for a specific circuit is to perform simulations of a balancing scheme according to [21] and out of that determine V_{FG} . When it has been determined, the circuit will be programmed and the value will normally be fixed during operation [21]. This method works for simulations only and can not be applied to fabricated circuits in order to determine V_{FG} .

The different types of PFG techniques we have found have been categorized and divided into four groups, see Table 1.

Table 1.

Type	References	Firstref. to in	Limitations
Resistive PFG (G1)	[9],[10],[11],[14] [22],[23],[24]	[11], 2002	DC offset, signal distortion [9]
Feedback PFG (G2)	[8], [13],[25], [26],[27]	[13], 2002	$V_{dd} > 2V_{th}$ [26], Leakage cur.[13]
Diode PFG (G3)	[28]	[28], 1998	Reverse diode leakage [28]
VCCS PFG (G4)	[29]	[29], 2004	Current leakage [29]

Group 1 consists of PFG circuits which have a resistive path connected to the FG-node. It can be created out of different types of elements but they all have in common that it should create a resistive connection to the FG-node when it is turned on [9],[10],[22],[23],[24]. A PFG with a resistive path can either be recharged by a clocked switch or be continuously turned on. Figure 2a shows a PFG with resistive path.

Group 2 is PFG designs with a feedback loop that will in some way recharge the floating node [8],[13],[25],[26],[27]. The feedback loop can also be clock controlled or continuously turned on like group 1. The PFG circuit we have designed within this work, described in the Simulations part, can be classified into group 2 since it uses a weak feedback buffer to retain the floating-gate charge. This is also shown in figure 2b.

Group 3 is a technique where you connect a reverse biased diode to the FG node, figure 2c [28], and in group 4, a voltage controlled current source (VCCS) is connected to enable a recharge of the PFG [29], see figure 2d.

Floating-gate circuits have the advantage compared to other digital design techniques that several of the basic logic functions (NAND, NOR, NOT) and a few other commonly used gates (i.e. CARRY') can be designed with only two transistors per gate together with a number of floating-gate capacitances representing the fan-in number [30]. This advantage is used in the simulations, and figure 2e) shows a minority-3 gate (threshold gate) in FGMOS that have been used as the basic building block in the circuit.

III.SIMULATIONS AND RESULTS

In the simulations for this work, a weak feedback loop was introduced to stabilize the floating-gate node [26]. The type of feedback being used can be seen in figure 2b and this is, as far as we have found, first referred to in [8]. The feedback will force the output to an equilibrium state when dc signals are applied on the input and the simulation results also shows that only input signals within a certain frequency band will give correct output values.

The FGMOS minority-3 gate and the FG-inverter should both work with subthreshold power supply according to previous research [15] and the fan-in of the circuit can be up to 5 while retaining functionality [17]. Even with these restrictions on the circuit, limitations of the performance are experienced. Even further restrictions must be applied if the EDP performance should be better than for CMOS so the chosen design for the simulations actually has a fan-in of 3. This is also a result from [17] (at 250 mV power supply) and the restriction in fan-in will also limit the FGMOS ADC to 2-bits instead of the 3-bits that would have been possible with fan-in 7 [18].

According to [26], this type of PFG circuits will not work properly when the power supply voltage is reduced below 2 times the transistor's threshold voltage, V_{th} . Due to this, the power supply is chosen to 1.00 V for the simulations.

The simulations of the PFG above have been performed in Cadence using the Spectre simulator. The process technology is 120 nm CMOS and the transistors are of low-leakage type with minimum gate lengths in the designs. The threshold voltage, V_{th} , for these low-leakage transistors are 383 mV for nMOS and -368 mV for pMOS.

Figure 3 shows the topology for the simulated circuit and Figure 4 shows the plot of a transient analysis when the circuit works as a frequency doubler. The topology is new for this type of PFG and it is designed in a similar way to a topology of 3-

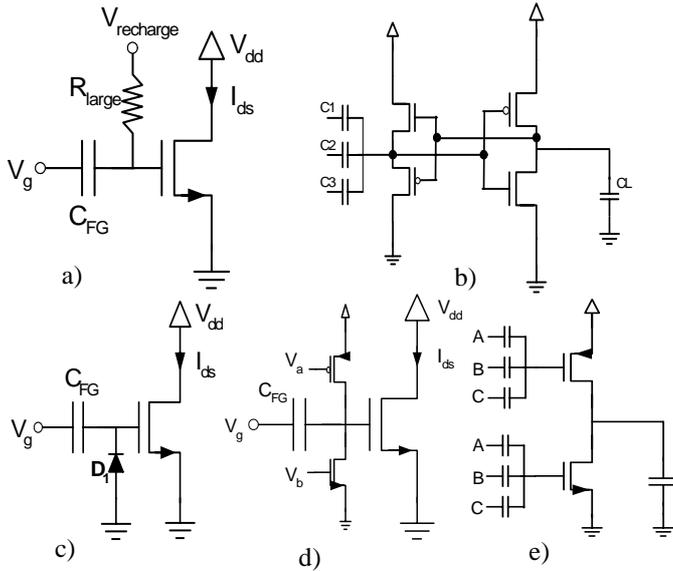


Fig. 2. a.) PFG with resistive load
 b.) PFG with feedback and fan-in 3
 c.) PFG with reversed diode
 d.) PFG with Voltage Controlled Current Source
 e.) Majority-3 Floating-gate with fan-in 3

bits ADCs used in [16], [18].

The transient analysis in figure 4 shows how the frequency doubling works. An input signal ramp with a certain switching period will generate a square output wave with the same frequency on the most significant bit of the ADC. At the same time a square wave with twice the input frequency will be generated on the least significant bit of the ADC.

IV. DISCUSSION

When the work with this paper started, the intention was to design and simulate a PFG ADC for subthreshold power supplies. During the design work problems and limitations were discovered that will make it harder to manufacture circuits with full functionality.

The circuit that have been designed and simulated does not necessary have to be used as a converter. It can in also be considered as a frequency doubler. With 2-bits output, the output can be doubled in frequency compared to an input ramp signal.

Performance for standard static CMOS will in reality probably be even better compared to FGMOS than this case of fan-in 3 because previous simulations have shown that FGMOS has most advantage for true floating-gate circuits [17],[19]. Introduction of PFG circuits will produce worse performance results than the more ideal true-FGMOS case, and at the end, the gain that can be achieved might not be worth the effort of redesign.

The dynamic behaviour that the ADC shows is another limiting factor. The circuit must be designed for specific input signal frequencies (limited bandwidth) and it will be a challenge for the designer if the frequency band for the applications should change. This will also require the design to change.

The equilibrium state that occurs for dc signals could be seen as a continuous leakage from the gates which indicate that feedback PFGs are not suitable for applications with static

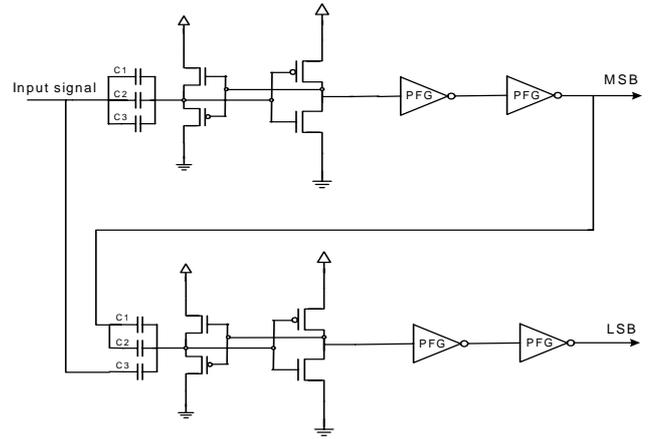


Fig. 3. A/D-converter (Frequency Doubler) designed with PFG fan-in 3 gates.

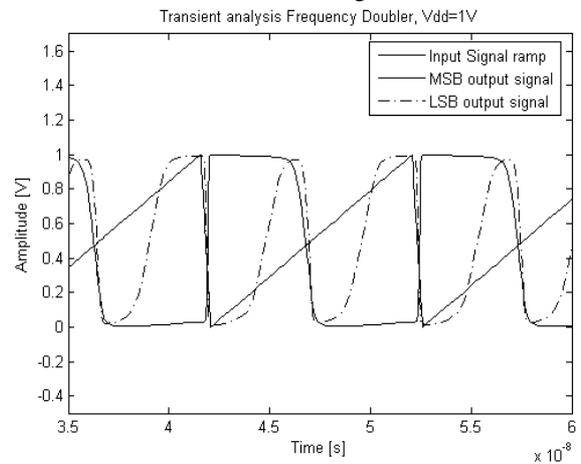


Fig. 4. Transient analysis of PFG ADC with input ramp signal. The output shows the frequency doubling input signals while normal floating-gate circuits generally works well even for these kinds of static dc signals.

The fact that input signals also must be clocked with a certain time interval in order to refresh the output signal values and avoid signals charge/discharge towards equilibrium is also limiting the performance and increasing power consumption.

The limiting factors that have been found for the other compared PFG groups are all related to current leakage at the floating-gate node because of the introduced programming ability. The circuits of group 1 will have dc offset, signal distortion and signal-dependent offset mainly caused by a slightly forward biased n-well/substrate junction diode connection [9]. Group 3 will be limited by leakage reverse current through the diode [28] and the feedback PFG in group 4 can have limitations because of reverse current through a PN junction of switching transistors [13].

V. CONCLUSIONS

Design and simulation of pseudo floating-gate circuits for subthreshold can be associated with several major limitations.

When it comes to fan-in, limitations shown from true floating-gate simulations says that a maximum fan-in of 3 is preferred even if the circuit might be functional with fan-in up to 5

[17]. This limitation might be so important for some circuits that most of the advantages in terms of speed and power consumption compared to standard static CMOS will be lost.

The power supply for PFG circuits might also be limiting for the design. Some PFG circuits, e.g. with feedback loop will have limitations that make them not suitable for subthreshold power supply and for those circuits the V_{dd} is required to be at least two times V_{th} like in the case of this work.

To summarize the work in this paper we conclude that it will most probably be possible to design a fully functional PFG circuits that have better speed or power performance than CMOS at subthreshold levels but in the end, the limitations of PFG circuits can make the design time very long and time consuming. In order to achieve the preferred performance it might not be worth the effort compared to make a standard CMOS design in many cases. The leakage currents from the FG-nodes through the connected refresh circuits will also be too large.

When future process technologies can offer new materials with lower current leakage through the gate and other improvements compared to what is state-of-the-art today, then it might be of a higher value to look into this PFG technique again. Until then, we can only recommend to carefully consider designs using pseudo floating-gate techniques for digital subthreshold designs and always do comparative simulations with standard static CMOS design.

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